Advanced Algorithms for Performance Monitoring in Synchronization Networks

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Abstract: - Advanced synchronization networks are provided with monitoring systems that allow verifying continuously, in real time, the performance achieved in timing distribution. In this paper, centralized and decentralized strategies for performance monitoring in synchronization networks are first outlined, by highlighting system architectures, advantages and drawbacks. Then, advanced algorithms for implementation in performance monitoring cards of state-of-the-art network clocks are proposed. The methods outlined in this paper allow the engineer to successfully cope with the issue of proactively monitor network synchronization performance, in order to detect timing degradations before they impact service.

Keywords: - clocks, digital communication, jitter, quality of service, synchronization, wander.

1 Introduction

Network synchronization has gained increasing importance in telecommunications throughout the last thirty years, especially since transmission and switching turned digital [1][2]. Actually, the quality of most services offered by network operators to their customers is affected by network synchronization performance. Digital switching, SDH (Synchronous Digital Hierarchy), ATM (Asynchronous Transfer Mode), GSM (Global System for Mobility), GPRS (Global Packet Radio Services) and UMTS (Universal Mobile Telecommunications Services) are striking examples where the availability of network synchronization references has been proven to affect quality of service.

The *synchronization network* is the facility implementing network synchronization. It provides all telecommunications networks served with reference timing signals of required quality. Most modern telecommunications operators have set up one or more synchronization networks to synchronize their switching and transmission networks.

Basic elements of synchronization network are nodes (autonomous and slave clocks) and links interconnecting them (e.g. copper cables, optical fibres, radio links). An *autonomous clock* is a stand-alone device able to generate a timing signal, starting from some periodic physical phenomenon. A *slave clock*, on the other hand, is a device able to generate a timing signal having phase (or much less frequently frequency) controlled by a reference timing signal at its input. Thus, slave clocks are usually realized based on the Phase-Locked Loop (PLL) scheme [3].

In the synchronization network standard architecture defined by ITU-T and ETSI [4][5], based on the Hierarchical Master-Slave (HMS) strategy, the network master autonomous clock is called *Primary Reference Clock* (PRC). Moreover, in very short, two types of slave clock are defined: the building clock synchronizing all equipment within an office building, called *Synchronization Supply Unit* (SSU) or *Stand-Alone Synchronization Equipment* (SASE), and the *SDH Equipment Clock* (SEC).

Advanced synchronization networks are provided with monitoring systems that allow verifying continuously, in real time, the performance achieved in timing distribution. The rationale of synchronization performance monitoring is the need to be *proactive*, i.e. to detect timing degradations well before they impact service.

There are several possible sources of severe timing impairments, such as maintenance activities, clock diagnostics and rearrangements, etc. Most of these phenomena yield abrupt phase hits on the timing signal, or even loss of it, and thus can be quite easily recognized. Nevertheless, being capable to detect promptly degradations such as slow frequency drifts or phase wander may be the key factor enabling to guarantee that the quality of service will be not suddenly affected at a later time. Such timing degradations are definitely not easy to diagnose with traditional alarm reporting systems. An advanced synchronization performance-monitoring system should be effective to automatically identify subtle synchronization problems before the service is affected.

2 Synchronization Hard and Soft Failures

Synchronization hard failures are those caused by equipment hardware outages (e.g., failures in micro-components, clock units, output cards, etc) or by cable outages, mostly caused by construction machines, which may damage the cables during road works. Most commonly, hard failures are detected by the downstream slave clock as *Loss of Signal* (LOS) or *Alarm Indication Signal* (AIS) alarms. Upon detecting a hard failure on the current

reference input timing signal, the slave clock should select an alternative reference signal or enter holdover mode. The slave clock should also report the hard failure to the network management system.
Possible causes of *synchronization soft failures*, on the other hand, are slow frequency drifts and excessive jitter and wander on the synchronization signals. For example, slow frequency drifts can be caused by timing loops, after inappropriate protection switching, or by intermediate transmission equipment entering holdover mode. Severe synchronization soft failures can yield occasional *Loss of Frame* (LOF) or slips at the input ports of transmission and switching equipment.
Subtle synchronization soft failures may be deceitful and not manifest themselves until they do not worsen enough to suddenly affect the traffic signals. Hence the need of an accurate synchronization performance-monitoring system, which enables the network manager to proactively identify synchronization problems and to solve them before service is affected.

3 Strategies for Synchronization Performance Monitoring

Performance monitoring of a synchronization network is based on *local* measurements of the timing performance, carried out in as many office buildings as possible. Advanced SASE clocks are equipped with performance-monitoring cards that compare the local timing signal to one or more external references, for measuring the phase error between them. Two kinds of external reference can be used for performance monitoring at a certain SASE clock:

- *terminated synchronization signals*, i.e. input timing signals terminating a synchronization trail at that node;
- *return synchronization signals*, i.e. timing signals transported back to the node from the far end of synchronization trails originating from the node.

The former kind of reference corresponds to a *decentralized strategy* of synchronization performance monitoring. Clocks located at terminal points of synchronization trails must be provided with performance-monitoring capability. The main advantages are that only one monitoring card is needed in each of those clocks, at least in principle, and that a failure in a monitoring node would not affect the monitoring capability of the rest of the network.
Conversely, the latter kind of reference corresponds to a *centralized strategy* of synchronization performance monitoring. Central clocks carry out performance measurements on return synchronization signals, as phase error with the local timing. In this case, the main advantages are that fewer clocks need monitoring capability and that return signals are monitored at a central location, by direct comparison to the reference they are supposed to trace.
It is evident that the centralized strategy allows recognizing rather easily synchronization network misbehaviours. If the central monitoring node detects synchronization impairments on a single return line, then it is reasonable to infer that the clock at the far end of that line is having problems. Conversely, should all the return lines exhibit synchronization impairments, then it is most likely that the central node reference is misbehaving.
Various examples of both strategies are shown in the scheme of Fig. 1. Therein, grey wide arrows indicate how synchronization propagates from the network master clock to slave clocks. Moreover, black arrows denote synchronization signals carried via some transport facility (e.g., 2.048-Mbit/s signals).

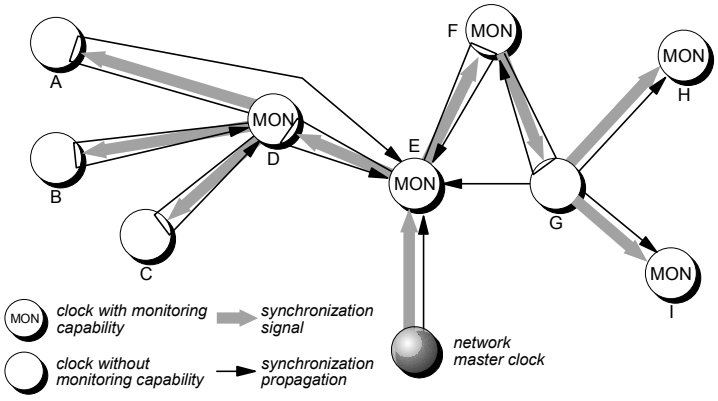

Fig. 1: Centralized and decentralized strategies for synchronization network performance monitoring.

Clocks marked with A, B, C and G are not equipped with monitoring capability. Clocks marked with D, E, F, H and I carry out performance monitoring: among them, clocks H and I perform measurements on terminated synchronization signals; clocks D, E and F perform measurements on return synchronization signals.
Monitoring return signals must not be done necessarily on signals returning from direct slave clocks in the timing distribution hierarchy: clock E monitors a return signal from clock D (direct slave) and a return signal from clock A (slave of clock D). Likewise, clock E monitors a return signal from clock F and a return signal from clock G (slave of clock F).

4 Algorithms for Synchronization Performance Monitoring

Comparing the local timing to the terminated synchronization signal (decentralized strategy) means to measure the phase or time error[1] between the input reference and the output signal of the SASE clock (as shown in Fig. 2a). On the other hand, comparing the local timing to a return synchronization signal (centralized strategy) means to measure the phase or time error between the SASE output signal and another external reference, which is supposed to trace the monitoring clock (as shown

1 The *phase error* $\Delta\varphi$ between two chronosignals is measured in [rad], often with the ambiguity of the number of full circles ($\Delta\varphi=\Delta\varphi+2k\pi$). The *time error* is measured in [ns] and has no ambiguity: it means the total delay of one timing signal compared to the other.

in Fig. 2b). Therefore, the performance-monitoring card in Fig. 2 should include the following basic functions:

- measurement and acquisition of time error data between the clock output signal and each of the reference signals;
- evaluation of standard synchronization quality quantities based on the acquired data sets, such as *equivalent slip rate*, *Time DEViation* (TDEV), *Maximum Time Interval Error* (MTIE) [6][7];
- communication with the synchronization network management system for performance reporting.

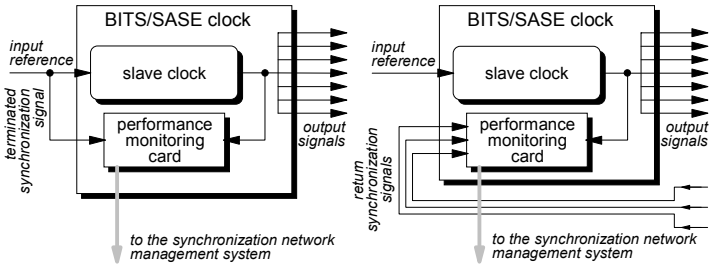

Fig. 2: Synchronization performance monitoring in a SASE clock according to a) decentralized and b) centralized strategies.

4.1 Monitoring the Terminated Synch Signal

In the scheme depicted in Fig. 2a, performance monitoring is carried out by measuring the time error between the input and the output of the local slave clock. This configuration is standardized as *synchronized-clock measurement configuration* by ETSI [6] and ITU-T [7]. Let

$$H(f) = \frac{\Phi_{\text{out}}(f)}{\Phi_{\text{in}}(f)} \tag{1}$$

be the low-pass transfer function of the PLL, where $\Phi_{\text{in}}(f)$ and $\Phi_{\text{out}}(f)$ are the Fourier transforms of the phase noise functions $\varphi_{\text{in}}(t)$ and $\varphi_{\text{out}}(t)$ on the input and output timing signals respectively, characterized by cut-off frequency f_c. Then, the most remarkable facts are that:

- the transfer function from the input phase to the input-output phase difference (measured according to Fig. 2a)

$$\frac{\Phi_{\text{in}}(f) - \Phi_{\text{out}}(f)}{\Phi_{\text{in}}(f)} = 1 - H(f) \tag{2}$$

  is high-pass, i.e. only high-frequency ($f>f_c$) phase noise from the input is revealed by measuring the input-output phase error;
- internal oscillator phase noise is transferred high-pass filtered to the output phase $\varphi_{\text{out}}(t)$ and thus also to the phase error $\varphi_{\text{in}}(t)$-$\varphi_{\text{out}}(t)$; phase noise from other internal sources such as the phase detector, on the other hand, is transferred to the output low-pass filtered.

Therefore, to give some empirical guidelines:

- by measuring the quantity $\varphi_{\text{in}}(t)$-$\varphi_{\text{out}}(t)$ according to the scheme of Fig. 2a, phase impairments present on the input reference and those generated by the slave clock itself are revealed mixed in the measurement results;
- for $f<f_c$, the slave clock is supposed to track input phase fluctuations; therefore, should slow phase changes be measured, they must be due to some clock internal misbehaviour (i.e., the slave clock is losing track and is generating the phase change);
- for $f>f_c$, the slave clock cuts off input phase fluctuations; therefore, should fast phase fluctuations such as steps or spikes be measured, they must be due most likely to the input reference line rather then to the local oscillator (i.e., the slave clock is commonly assumed to work correctly, whereas the upstream clock does not).

4.2 Monitoring Return Synchronization Signals

In the scheme depicted in Fig. 2b, performance monitoring is carried out by measuring the time error between the output of the monitoring clock and a few return synchronization signals, coming from remote lower-level nodes that are synchronized by it, directly or indirectly.

As in the previous case, generally it is not possible to distinguish unambiguously whether phase impairments revealed in the results are due to the local oscillator or to some lower-level clock in the downstream chains, from whose far ends return synchronization signals come back.

Nevertheless, as already mentioned before, the availability of several return synchronization signals allows applying a sort of majority voting in interpreting measurement results. Reasonably, if a single return line exhibits impairments, then that slave clock chain will be assumed to misbehave; conversely, should all the return lines exhibit impairments, then the local clock will be probably assumed to misbehave.

Also in the scheme of Fig. 2b, measurements are carried out according to the synchronized-clock measurement configuration [6][7]. In this case, the input and the output of a lower-level clock chain, slave of the local clock, are compared. Analogous considerations as before can be thus made, yielding the following empirical guidelines:

- phase impairments generated by the local clock and by lower-level clocks result mixed in the measurements; nevertheless, majority voting can help to interpret results;
- for $f<f_c$, the slave clock chain is supposed to track phase fluctuations generated by the local clock; therefore, should slow phase changes be measured, they must be due to some downstream misbehaviour;
- for $f>f_c$, slave clocks cut off input phase fluctuations; therefore, should fast phase fluctuations such as steps or spikes be measured *on a single* return line, they must be due most likely to some clock on the trail from where that line comes back; should phase fluctuations be measured *on all* return lines, they must be due most likely to a local clock misbehaviour.

4.3 Evaluating the Equivalent Slip Rate

The performance-monitoring card acquires time-error data, measured between its input signals, and then evaluates some

quantities for synchronization quality assessment, such as equivalent slip rate, TDEV and MTIE [6][7].

Estimating the *equivalent slip rate* between two timing interfaces means to evaluate, by suitable algorithms, the controlled-slip rate that would be detected should that two timing signals be used to drive the write and read processes in a bit-synchronizer buffer. The value of such a slip-monitoring feature is thus to emulate the possible effect of measured phase impairments on the operation of an actual network.

Monitoring and counting slips occurred on digital interfaces of switching exchanges is *reactive*, as we record data loss when it is already happened. Measuring the time error among several, strategically chosen couples of nodes in the network and assessing the equivalent slip rate is *proactive* instead, because it provides a more general view of the network synchronization status: all nodes are under control if a good monitoring strategy is planned. Therefore, we are warned also about slips that *may* occur, should we feed a digital switch with signals coming from any two nodes of the network.

An algorithm for equivalent slip rate estimation evaluates, over certain time intervals, the expected number of controlled slips on a given timing interface between two primary rate digital signals. That is, given time-error data measured between two timing signals, the operation of an elastic store is emulated, in order to count the number of controlled slips that would occur, over certain time intervals, by using that timing signals for reading and writing.

If time error is dominated by sole frequency offset, after an initial transient the slip rate does not depend on the initial buffer fill level neither on the hysteresis value. The slip rate F_{slip} is function of the number N of bits repeated or lost in one slip (obviously, the buffer size can not be smaller than $2N$) and of the frequency offset $|f_w-f_r|$ between writing and reading processes. Expressing the frequency offset in [Hz], the following simple relationship holds

$$F_{\text{slip}} = 86400 \frac{|f_w - f_r|}{N} \quad [\text{slips/day}] \qquad (3)$$

where 86400 is the number of seconds per day.

Nevertheless, when jitter and wander dominate, as between input and output of a system of slave clocks, the initial buffer fill level and the hysteresis value should be kept into account in emulating accurately the behaviour of actual buffers. A possible way to deal with the issue of the initial phase alignment in performance-monitoring cards is to emulate a set of multiple slip buffers, each with different initial fill level, uniformly chosen within the entire threshold spacing (equal to one PCM frame length, i.e. 125 μs in time units). For example, emulating an initially empty buffer and an initially full buffer yields the limit values of the slip rate. As far as the hysteresis value is concerned, ITU-T Recs. G.823 and G.824 [7] specify a minimum value of 18 μs. More details on algorithms for evaluating the equivalent slip rate can be found for example in [2].

5 Conclusions

In this paper, centralized and decentralized strategies for performance monitoring in synchronization networks were outlined, by highlighting system architectures, advantages and drawbacks.

Then, advanced algorithms suitable for implementation in performance monitoring cards of state-of-the-art SASE clocks were proposed. Empirical guidelines were provided to allow the engineer to distinguish between phase impairments present on the input reference and those generated by the slave clock itself, which appear mixed in the measurement results. Finally, the issue of evaluating the equivalent slip rate was addressed.

The methods and algorithms outlined in this paper allow the engineer to successfully cope with the issue of proactively monitor network synchronization performance, in order to detect timing degradations before they impact service.

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