Jitter Testing Technique and Results at VC-4 Desynchronizer Output of SDH Equipment

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Abstract— **Specifications relative to jitter and wander generation, at the output of desynchronizer systems, represent one of the hottest topics in characterizing SDH equipment. Among the many factors involved, pointer adjustments, due to phase deviations between the received timing signal and the SDH equipment internal clock, play indeed a primary role in phase noise accumulation. This paper deals with two different kinds of test designed for measuring—from 0 Hz on—phase transients due to AU pointer adjustments, namely: static and dynamic jitter measurement configuration. Moreover, results obtained by applying this technique to different suppliers' equipment are herein presented.**

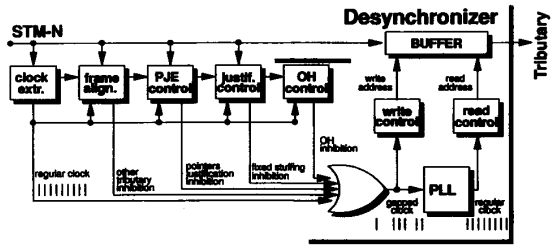

Fig. 1. Desynchronizer logical scheme.

I. Introduction

JITTER, i.e., the instantaneous phase deviation between a real and the ideal digital signal, represents one of the most important parameters in the characterization of telecommunications systems, because of its high influence on the transmission quality. The introduction of SDH [1], [2] networks requires new jitter specifications, and consequently new measurement techniques to achieve satisfactory network performance control. For SDH equipment with Plesiochronous Digital Hierarchy (PDH) [3] tributaries, Rec. G.783 [2] details output jitter specifications for PDH interfaces, due to the combined effect of tributary mapping and pointer adjustments.

While other jitter measurement techniques for SDH equipment—viz. those for jitter tolerance and jitter transfer function—are similar to those for PDH equipment and thus well consolidated, little work has been done so far on test methodologies for measuring the jitter affecting the PDH signal at the output of SDH apparatuses. This paper deals with the study of the output jitter at a 139.264 megabit/s port in the SDH Line Terminal STM-16 (LT-16), for which two different test methodologies are proposed.

II. Jitter Sources at PDH-SDH Boundaries

A. Tributary Mapping into the SDH Structures

The adaptation process of PDH tributaries into SDH structures, as defined in [1], results in one of the biggest technical challenges in designing SDH equipment. The insertion of a plesiochronous tributary into the corresponding synchronous Container (C) is accomplished by the *synchronizer* system. Bit justification accommodates frequency deviations of the PDH tributary from the nominal value.

At the receiver side, the PDH tributary is extracted from its C by the *desynchronizer* system (see Fig. 1). Here, the output "mapping jitter" is mainly due to two different sources. First, the irregular spacing of tributary bits in the SDH frame leads to some jitter in the demapped signal. In fact, as shown in Fig. 1, the STM-N signal clock has to be gapped to eliminate all bits not belonging to the tributaries (fixed stuffing bits, justification opportunity bits, overhead bytes). The read clock used to generate the output signal is rebuilt from the gapped clock by a Phase-Locked Loop (PLL), or a more sophisticated circuit implementing special algorithms. The low-frequency jitter caused by these gaps is not completely deleted by the desynchronizer, and therefore is still present in the output signal. In literature [4], [5] this low-frequency jitter is sometimes called *wander* (i.e., jitter at $f < 10$ Hz). However, for the sake of simplicity, the name jitter will be used to refer to wander as well.

The second source is the process due to the waiting time [6] between the instant of the justification decision and the instant in which the opportunity bit occurs, and was already well known for PDH systems too.

B. Pointer Adjustments

Pointers give the position of *Virtual Containers* (VC) [1] in the STM-N frame, and are placed in a fixed position in the SDH frame structure. They allow payload fluctuations: when the phase offset between the output frame structure and the VC in the incoming frame exceeds a certain threshold, the VC in the output frame is moved backward or forward and the pointer value is updated accordingly. This process is called *pointer adjustment*. Three bytes are involved in AU-4 positive or negative pointer adjustments: when the VC-4 is moved backward, three additional bytes in the overhead field

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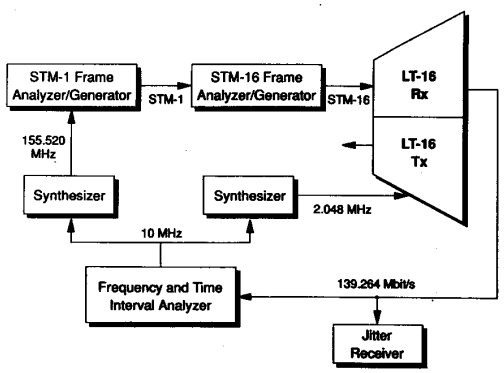

Fig. 2. Static jitter test bench.

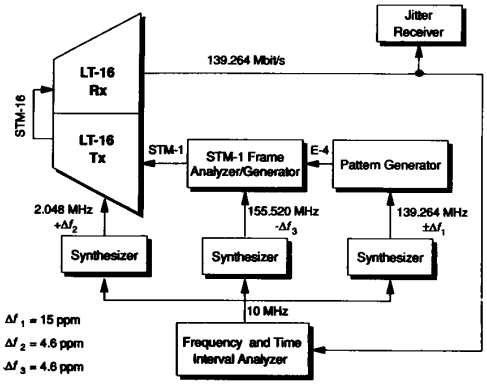

Fig. 3. Dynamic jitter test bench.

of the STM-N frame (*negative justification*) are filled; when it is moved forward, three bytes of the payload matrix are emptied (*positive justification*).

The main consequence of pointer adjustments consists of an additional contribution to the output jitter of demapped tributaries. In fact, in the sample case considered, each AU-4 pointer adjustment generates a 3-byte phase shift (24 UI), which is low-pass filtered by the desynchronizer and so smoothed to the output.

III. Jitter Testing Techniques

Two different techniques for measuring SDH desynchronizer output jitter are proposed in the following subsections. Measurements are performed in the absence of input jitter, and therefore the output jitter is only due to SDH mapping and to pointer adjustments. Both techniques measure the peak-to-peak (pk-pk) output jitter, thus allowing an easy comparison with values recommended in [2]. The tests reported relate only to the "combined case" [2], with the other one the same as for the old PDH measurement.

A. Static Jitter Measurement Configuration

As the first measurement technique (*static jitter measurement*) is concerned, the pointer activity is stimulated as different pointer test sequences defined in [2]. In Fig. 2 the test bench for the LT-16 is depicted. Both the Equipment Under Test (EUT) and the test instruments are synchronized via two synthesizers by the same master clock, an Oven-Controlled Crystal Oscillator (OCXO) contained inside the Frequency and Time Interval Analyzer. The STM-1 signal, containing a VC-4 mapping a plesiochronous 139.264 megabit/s, is generated updating the AU-4 pointer according to the sequences proposed in [2]. This STM-1 signal is then inserted in the STM-16 frame and sent to the LT-16, whose desynchronizer extracts the 139.264 megabit/s plesiochronous signal. The Frequency and Time Interval Analyzer displays the jitter as a function of time by comparing the phase of the desynchronizer output signal with the phase of an internally synthesized 139.264 MHz clock. A Jitter Receiver allows measuring jitter in the frequency bands specified by [2].

The capability to stress the desynchronizer with repetitive same-sign pointer adjustments, or repetitive alternate positive and negative pointer adjustments, allows the exact determination of desynchronizer operating limits. Results are reported and discussed in Section IV.

B. Dynamic Jitter Measurement Configuration

The second measurement technique (*dynamic jitter measurement*) is mainly based on pointer actions caused by a frequency offset between the EUT clock and the clock of the incoming signal, in opposition to the previous case where justifications were directly imposed by the testing instrument in a "static" way. This configuration aims to simulate the stress at PDH-SDH boundaries when some equipment clock is in "free-running mode."

The test bench is depicted in Fig. 3. Also here, the Frequency and Time Interval Analyzer works as master clock. Three synthesizers supply frequencies with offset values selected to test the worst case admitted by relevant Recs. [7], [8]. In this way the EUT must compensate with pointer adjustments the total clock offset of 9.2 ppm. The Frequency and Time Interval Analyzer displays the jitter as a function of time by comparing the phase of the desynchronizer output signal with the phase of an internally synthesized clock at the same frequency (139.264 MHz + 15 ppm) of the Pattern Generator. A Jitter Receiver allows measuring jitter in the frequency bands specified by [2]. Results are presented and discussed in the next section.

IV. Measurement Results

Some results of static and dynamic jitter measurements are herein presented. These measurements have been accomplished in the frame of an experimental field trial, where several LTs-16 supplied by different vendors have been tested [9].

As static testing is concerned, Fig. 4 shows the 139.264 megabit/s tributary jitter waveforms. Each of these plots displays the results obtained, on the same piece of equipment, with each of the pointer test sequences defined in [2] and depicted in Fig. 5. The desynchronizer smooths the shape of phase hits because of its low-pass effect. On the other hand,

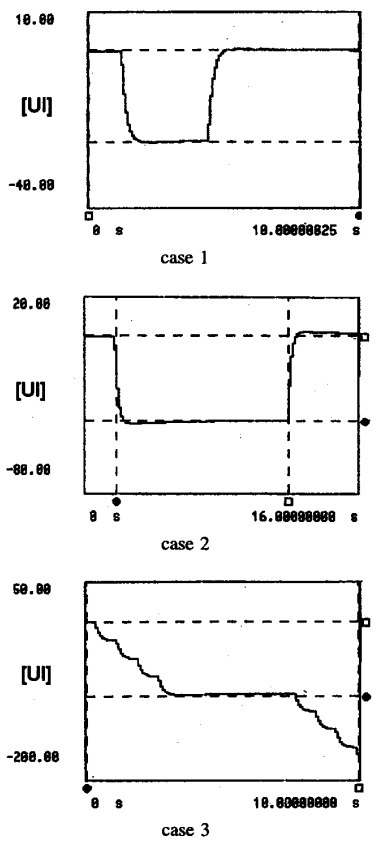

Fig. 4. Tributary jitter waveforms (static testing).

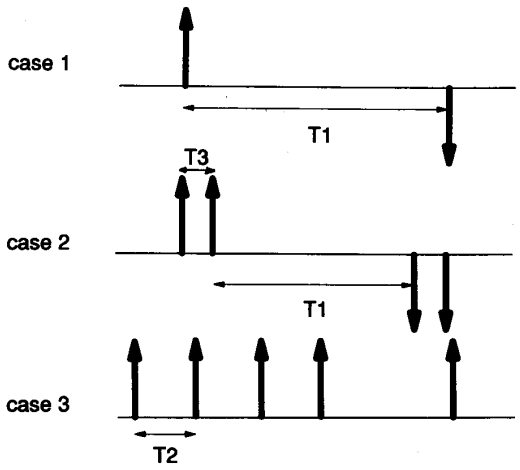

Fig. 5. Pointer test sequences.

the 139.264 megabit/s tributary jitter waveform measured in the dynamic testing configuration, on a different supplier piece of equipment, is displayed in Fig. 6 for an observation time of 100 s.

Eventually, the peak-to-peak jitter results, measured by the Jitter Receiver with the band-pass filters B1 (200 Hz–3500 kHz) and B2 (10 kHz–3500 kHz) defined in [10] and with a high-pass filter HPF (from 2 Hz on), are also shown in Table I for pure mapping (no pointer action) and both static and dynamic testing.

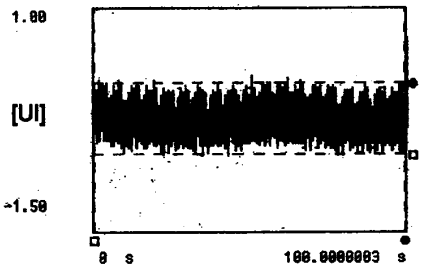

Fig. 6. Tributary jitter waveform (dynamic testing).

TABLE I
TRIBUTARY FILTERED JITTER MEASUREMENT RESULTS

Test	$B1[UI_{pk-pk}]$	$B2[UI_{pk-pk}]$	$HPF[UI_{pk-pk}]$
mapping	0.037	0.022	0.035
static (case 1)	0.038	0.027	0.049
static (case 2)	0.037	0.029	0.049
static (case 3)	0.038	0.028	1.797
dynamic	0.065	0.025	0.606

V. CONCLUSIONS

This paper deals with the measurement of the output jitter at the 139.264 megabit/s port of the SDH equipment. Two testing methodologies are proposed, and some measurement results are also shown. It is worthwhile noticing, from the measurement results shown in Table I, that most of the spectrum of jitter due to pointer adjustments is at low frequencies. This issue should deserve deeper consideration by standard bodies, since the results herein shown were obtained on an EUT in stand-alone configuration, and such wander may accumulate along the network with a dramatic impact on the quality of transported circuits.

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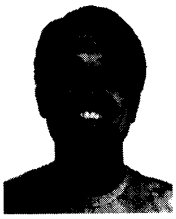

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