SDH Equipment Testing: an Italian Experience towards Standard Test Specifications

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Abstract — Managing world spreading of Synchronous Digital Hierarchy technology, nowadays and even more in the future, implies having extensive standard test procedures. SIRTI, on behalf of the Italian long distance operator IRITEL, tested STM-1 Add Drop Multiplexers and STM-16 Line Terminals provided by four different suppliers. The field-trial covered detailed testing of equipment. This paper details the test procedure we accomplished in order to fully check the functions of a single equipment. The most significant measurement set-ups are outlined, and some of the most interesting results are also shown. The test set herein presented is an attempt to build a first core of measures towards the future indispensable developing of standard test specifications.

I. Introduction

Synchronous Digital Hierarchy (SDH), defined in [1], is nowadays a well known trasmission standard, and its deployment in the most advanced networks has become a reality. In few years a massive introduction of SDH equipment is expected, together with completion of ITU-T Standards and related new equipment generation marketing. To manage such challenging scenario, with the complexity and the technical issues of such innovative equipment, standard test procedures are needed for two major applications: conformance testing and maintenance.

This paper covers and illustrates the conformance test set, and the measurement methodology, SIRTI developed for characterizing and evaluating STM-1 Add Drop Multiplexers (ADM-1) and STM-16 Line Terminals (LT-16) in stand-alone configuration, equipped with Optical Fibre Amplifiers (OFA), and supplied by four different factories to the Italian long distance operator IRITEL. This test set is an attempt to build a first core of measures towards a future standard characterization and evaluation of new equipment. Anyway, it can represent only the first step in achieving this goal, because future standard test specifications will stem from different hands-on experiences and new network requirements. In the following, the SDH field trial, in the frame of which testing was performed, is first introduced. The SDH equipment test procedure we accomplished is then described: the most significant measurement set-ups are outlined, and some of the most interesting results are also presented.

II. The SDH Field Trial

SIRTI, on behalf of the Italian long distance operator IRITEL, led a nine months field trial with the goal of characterizing the domestically available SDH equipment first in a stand alone configuration, and then connected as in multi-vendor networks. The trial began in April 1992. Four usual suppliers of IRITEL deployed everyone one ADM-1 and one LT-16 equipped with OFA. OFA applications are very important in Italy, owing to the long and narrow shape of the country, and to the fact that the average distance between the trunk offices is in the range of 80 Km and more. The environment in which the equipment were tested was the most realistic: a long distance office in Milan, where equipment were installed and connected using the optical fibre deployed in the city area. The results achieved in these trial were used by the operator for planning the future deployment of the long distance SDH network.

III. SDH Equipment Test Procedure

This section describes the conformance test procedure we accomplished. This procedure was approved by the national certification body ISPT (*Istituto Superiore delle Poste e Telecomunicazioni*) and aims to comprehensively check all the functions and interfaces of an Equipment Under Test (EUT). According to our experience, a comprehensive test procedure should carefully check at least the following main aspects:

- optical and electrical physical interfaces,
- correctness of the OverHead (OH) bytes generated by the EUT and possible EUT misbehavings owing to different values of input OH bytes,
- error free transport of payloads through anyhow cascaded input/output ports,
- time performance measures for Automatic Laser Shutdown (ALS) and Automatic Protection Switching (APS),
- frame alignment performance,
- pointer processor performance,
- synchronization unit performance,
- jitter and wander performance at input/output ports,
- alarms, performance, configuration management.

For lack of space, in the following subsections only the most innovating tests are discussed in detail. Other important ones, strictly related to equipment conformance testing, are OFA and power supply tests, but a detailed discussion of these topics is beyond the scope of this paper.

A. Optical and Electrical Physical Interfaces

The optical and electrical physical interfaces of SDH equipment are respectively specified in ITU-T Recommendations G.957 [2] and G.703 [3]. The purpose of this set of measurements is thus to verify the compliance of EUT physical interfaces to those requirements. Since physical interface testing techniques are very well established in the telecommunication industry, we will not spend more words about that.

B. OverHead Bytes

OH bytes testing can be logically split in two different phases: checking the correctness of OH bytes in the frames generated by the EUT, and checking possible EUT misbehavings owing to different values of input OH bytes.

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While the first is a *passive* check, where the EUT operates in normal conditions and we simply read the OH bytes coming out from output ports, in the second we play an *active* role: we feed the EUT with frames containing different test values in OH key bytes, and we read the output frames back observing possible EUT misbehavings.

As regards the first phase, the values in all SOH and POH meaningful bytes were checked if they matched with values specified in Rec. G.708 and G.709 [1]. As regards the second phase, the key octets are the communication bytes, special bytes like Z1-Z5 and other carrying alarm indication signals like K1, K2. It is worth remarking that unusual values in some bytes of the OH matrices gave rise to unexpected alarms in the EUT, though these bytes should have been not significant.

C. Error Free Transport of Payloads

This is the basic feature of any telecommunication equipment. Therefore, careful tests were accomplished under different operation conditions, e.g. under variations of the nominal frequency of tributaries. In one of these tests, for example, a E1 signal (2.048 Mbit/s), with variations of the nominal bit rate, was mapped/demapped 63 times through the cascaded input/output ports of an ADM-1. Conversely, the payload was also generated and mapped in a VC by a SDH Frame Generator/Analyzer linked to a synchronous port of the EUT. No problems were detected carrying out this group of tests.

D. Time Performance Measures for ALS and APS

Due to the very high power levels involved in SDH line systems, especially if equipped with OFA, a protection mechanisms (ALS) is likely to be required by standard bodies, in order to ensure human safety in case of cable break. In fact the laser safety problem has already been considered for SDH equipment, though not equipped with OFA, and an automatic shut-down and restart procedure is given in ITU-T Rec. G.958 [4]. However, no standard testing methods has so far been proposed to check the correct operation of this mechanism. Since a detailed discussion of this topic is beyond the scope of this paper, we refer the reader to [5], where the testing procedure we accomplished is fully described.

APS test was also performed both on LT-16 and ADM-1, but a detailed description of these tests is not possible for lack of space.

E. Frame Alignment Performance

Rec. G.783 [6] specifies the requirements for the frame alignment algorithm of a Synchronous Equipment (SE). The resulting state diagram is depicted in Fig. 1. Three states are defined: In Frame (IF), Out Of Frame (OOF), Loss of Frame (LOF). Indeed, Rec. G.783 does not specify what subsets of bytes A1, A2 may be used by the alignment algorithm, thus not constraining designers to a particular implementation. Therefore, frame alignment algorithm testing was done by finding out an answer to the following questions:

- what is the alignment word subset checked during normal *IF operation*?
- what is the alignment word subset checked during *alignment recovery* process?
- are the transition conditions between states of diagram in Fig. 1 compliant with constraints specified in G.783?
- is the implemented algorithm robust enough against high Bit Error Rate (i.e., BER=10^{-3}) affecting incoming frames?

The test procedures consisted in sending to the EUT suitable sequences of frames with wrong values in different locations in the alignment word. The EUT status was inferred by alarm monitoring or, better, by probing the OOF logical state *inside* the EUT if it is not directly accessible. In a very analogous way, the multi-frame alignment algorithm (H4 bytes) can also be checked.

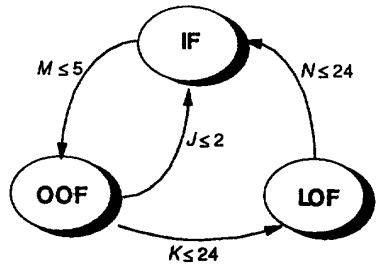

Fig. 1: Frame alignment state diagram specified in Rec. G.783

Testing of different suppliers equipment led to the following interesting results:

- during IF operation, most equipment just check the 8 central bits in the alignment word *N*×3×A1, *N*×3×A2 of the STM-*N* incoming frames (*N*=1, 4, 16);
- during alignment recovery process, most equipment look, along the incoming raw bits, for some consecutive bytes containing the hexadecimal word F6h (A1), and then for the couple F6h, 28h (boundary between A1s and A2s);
- the implemented algorithm proved compliant with G.783 [6] performance requirements.

F. Pointer Processor Performance

The requirements for the AU and TU pointer processor algorithm are specified in Rec. G.783 [6]. The resulting state diagram is depicted in Fig. 2. Three states are defined: normal operation, Loss of Pointer (LOP), Alarm Indication Signal (AIS). Here the key test topics are:

- check of payload error free transport under different pointer adjustment rates,
- check of the majority voting rule in interpreting the inversion of I and D bits in pointer word,
- check of the transition conditions between states of diagram in Fig. 2.

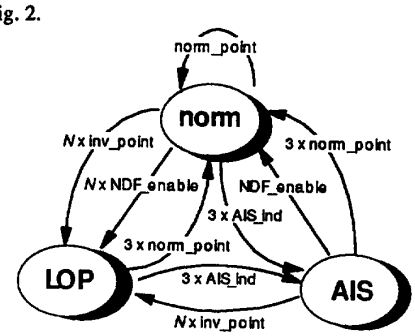

Fig. 2: Pointer processor state diagram specified in Rec. G.783

Special care was taken in synchronizing all the SDH nodes (if more than one) involved in this test, to provoke pointer actions only where and when we really want. A sample test bench is depicted in Fig. 3. Here, the SDH instrument generates frames with programmed sequences of pointer adjustments, and checks the payload back from the EUT (a LT-16). Testing of different suppliers equipment led to the following interesting results:

- the limit rate of one AU pointer adjustment every four frames, specified in G.783 [6], can be managed by SEs only if justifications are of alternate sign;
- indeed, the maximum rate of same sign AU pointer adjustments (e.g., all positive), manageable in incoming frames, is in the order of one hundred per second; beyond that, the buffers in desynchronizers overflow.

Anyway, it must be noticed that a rate of one hundred AU pointer adjustments per second corresponds to a frequency offset approximately equal to 15 ppm, well above the limit of 4.6 ppm specified in Rec. G.81s [7]. Analogous considerations hold for TU pointer justifications too.

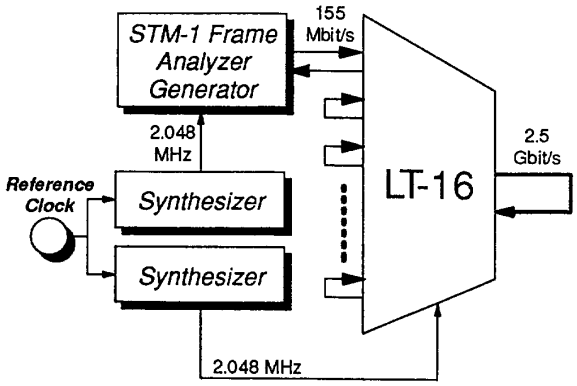

Fig. 3: Pointer processor testing on a STM-16 Line Terminal

G. Synchronization Unit Performance

Synchronization is a key function in SDH equipment. Therefore, special care should be taken in testing the EUT synchronization unit, in standards [8] also called Synchronous Equipment Clock (SEC), and basically consisting in a Digital Phase Locked Loop (DPLL) [9]. A comprehensive SEC test procedure is quite complex: it should comprise at least the long term frequency stability in hold-over operation, the phase hits on the output signal owing to reference timing source switching, the jitter transfer function, and the most advanced frequency stability measurements too (e.g. MTIE, Allan Variance, TVAR, TIErms).

All these tests were accomplished, in order to achieve the best characterization of SECs also beyond the scope of current standards. Since a detailed description of all these tests would be itself a subject for some papers, we will just spend some words on the last two, giving some directions and showing some of the most interesting obtained results.

1) Jitter Transfer Function - This measure was done directly on the G.703 [3] timing input and output signals (sine waves at 2.048 MHz). The test bench is depicted in Fig. 4: a timing signal affected by sinusoidal jitter at a given frequency is input to the EUT as reference timing signal, and the time counter measures then the jitter affecting the output timing signal. More details on the low frequency jitter measurement technique can be found in [17]. A sample of the measured results is shown in Fig. 5, which depicts the jitter transfer function measured on a LT-16. It is a single pole low pass function, with a slope of 20 dB/decade and a cut-off frequency around 5 mHz.

2) Advanced Frequency Stability Measurements - According to last directions in evolving ITU and European standards G.81s [7] and ETS DE/TM-3017 [8], frequency stability assessment of clocks in SDH networks is based on time domain measurement of the phase deviation of the chronosignal generated by the Clock Under Test (CUT), with respect to a reference clock.

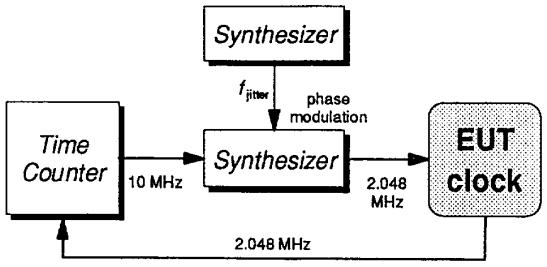

Fig. 4: Jitter transfer function measurement

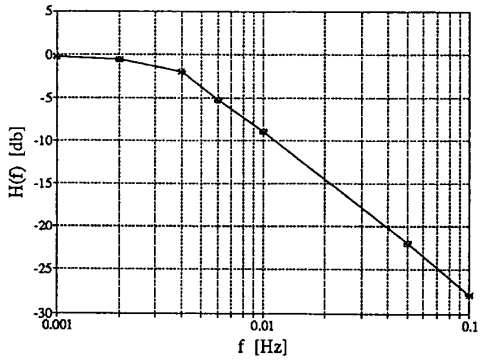

Fig. 5: Jitter transfer function measured on a STM-16 Line Terminal

Sequences of samples $\{x_i\}$ (i=1..N) spaced τ_0 seconds, of the Time Error process $x(t)$, are measured and stored for numerical post-processing, where samples x_i are the measured time intervals between two corresponding zero-crossing of the chronosignals generated by the CUT and the reference clock (see Fig. 6).

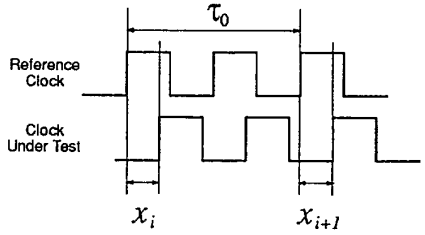

Fig. 6: Time Error measurement and sampling

Typical choices may be $N \cong 10^5$ and τ_0=0.1+1 s. Obviously, a key role is played by the resolution and the accuracy of the employed time counter: in our case, the resolution was 200 ps, while the measurement error noise floor was well below the measured values.

Basing on the sequence of measured values $\{x_i\}$, many quantities for clock frequency stability assessment are defined in literature [10][11][12][13][14]: among them, Maximum Time Interval Error (MTIE), Allan Variance, Modified Allan Variance, Time Variance (TVAR) and the root mean square of Time Interval Error (TIErms) are the most considered in telecommunications standard bodies, and therefore they were all computed. In Fig. 7, as an example, we show the Time Deviation

TDEV (square root of TVAR) and TIErms curves measured on an ADM-1 clock operating in slave mode. TDEV and TIErms were computed starting from a sequence of N=80000 samples x_i spaced τ_0=22 ms, thus spanning a measurement period T≅1800s. More details on properties of the quantities mentioned in this subsection, their evaluation based on Time Error measurement and related issues are available in references [15][16].

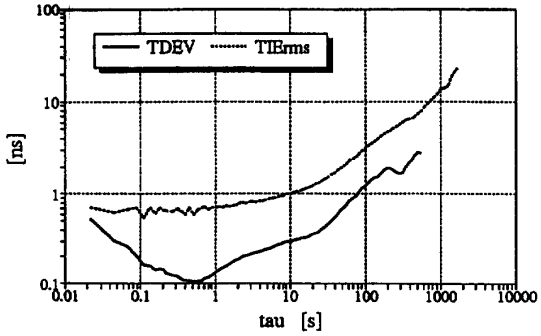

Fig. 7: TDEV and TIErms measured on a STM-1 Add Drop Multiplexer clock operating in slave mode (N=80000 τ_0=22 ms)

H. Jitter and Wander Performance at Input/Output Ports

Most part of these tests come directly from traditional Plesiochronous Digital Hierarchy (PDH) world: output jitter, maximum input jitter, jitter transfer function at the tributary ports are concepts well known to any telecommunication engineer. What's new, in SDH, is that jitter and wander at the output of desynchronizers are mainly due to two different causes: mapping of tributaries into the SDH structures, and AU and TU pointer adjustments.

Therefore, accurate desynchronizer performance assessment was accomplished, under different mappings and sequences of pointer adjustments. The technique we conceived, for measuring tributary wander at the desynchronizer output, is exhaustively described in [17], where some measurement results are also provided.

I. Alarms, Performance, Configuration Management

Neglecting the Telecommunication Management Network (TMN) and Q interfaces (see G.784 [18]), every SDH equipment is locally controlled by a workstation running proprietary software, which provides alarm reporting, performance monitoring and configuration management. Through this interface, the main items that were checked are the quality and completeness of alarm, performance and configuration reporting, the alarm consequent actions (specified in G.782 [6]), the number of available performance parameters (specified in G.826 [19] and G.784 [18]), the flexibility in setting thresholds of those parameters and in configuring connection matrices of VCs, and any extra feature provided by the EUT though not mandatory.

IV. CONCLUSIONS

Managing world spreading of SDH technology, nowadays and even more in the future, implies having extensive standard test procedures. This paper detailed the test procedure SIRTI accomplished, on behalf of the Italian long distance operator IRITEL, in order to fully check the functions of Add Drop Multiplexers STM-1 and Line Terminals STM-16. The most significant measurement set-ups were outlined, and some of the most interesting results were also shown. The test set herein presented is an attempt to build a first core of measures towards the future developing of standard test specifications.

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