Preliminary Experimental Results for the Development of the new Italian Synchronization Network

Roberto Bonello†, Stefano Bregni°, Marco Carbonelli*, Antonio Manzalini†, Alfonso Mariconda**, Domenico De Seta*, Daniele Perucchini*, Luca Valtriani††

†CSELT, Via G. Reiss Romoli 274, 10148, Turin, Italy
°CEFRIEL, Via Emanueli 15, 20126 Milano, Italy
††Sirti S.p.A., R&D - Network Technologies Div. Via A. Manzoni 44, 20095, Cusano Milanino, Italy,
*Fondazione Ugo Bordoni , Via B. Castiglione 59, 00142 Rome, Italy,
**TELECOM Italia, Via della Vignaccia 45, 00100, Rome, Italy

Abstract

In the development of SDH transport network, the availability, within each network node, of synchronization reference signals satisfying stringent stability requirements is fundamental for the operation of synchronous equipment at the desired quality level. Hence, it becomes necessary to implement a new advanced synchronization network able to filter and distribute high quality timing reference. In order to correctly design such a synchronization network it is useful, preliminarily, to characterize the timing performance of both presently used synchronization networks and timing units of existing digital equipment.

In this paper, results of measurements carried out on digital exchanges of the Italian network, SDH equipment clocks and stand-alone synchronization units are reported and discussed. Moreover, PDH link ability to transport timing reference has been investigated in order to verify the possibility of utilizing such links for the transport of timing signals of the new synchronization network .

1. Introduction

The widespread penetration of digital techniques for transmission and switching in Telecommunication Networks, which took place during the last fifteen years, made it necessary to distribute in each network's node timing references suitable for synchronization of digital exchanges and plesiochronous 1/0 cross-connects; as a consequence, in the same period, all the major PNOs (Public Network Operators) developed synchronization networks using various architectures, generally based on the master slave strategy, and, in the majority of the cases, trying to minimize the amount of stand-alone, specialized equipment installed for synchronization purposes.

By the end of the 80's, a new generation of digital systems based on SDH (Synchronous Digital Hierarchy) and ATM (Asynchronous Transfer Mode) has been developed; in the near future these systems will be gradually introduced in Telecommunication Networks to improve network availability and flexibility, as well as to ensure the provisioning of broadband, high quality services. Obviously, the new systems will be required to guarantee complete backward compatibility with existing systems (e.g., transmission plesiochronous systems).

Focusing the attention on issues related to the introduction of SDH systems and to the compatibility with PDH (Plesiochronous Digital Hierarchy) systems, it is a common understanding that SDH equipment need a very high performing synchronization distribution network in order to limit, as far as possible, pointer processor activity. In fact, excessive pointer activity on an SDH link has a strong impact on the jitter and wander affecting transported PDH tributaries and, consequently, on the quality of transported services. In order to reduce jitter and wander levels it is necessary to make available, at SDH nodes, synchronization reference signals showing very stringent short term phase noise stability performance [1,2] together with a good long term stability [3]. These performance can be obtained adopting for the synchronization distribution network the hierarchical Master-Slave [4] architecture and using an atomic (Cesium) oscillator as PRC (Primary Reference Clock) together with Rubidium or quartz crystal oscillators for both transit and local synchronization network nodes.

In normal operation, all the node clocks are traceable to the PRC: in this condition each node clock is required to reduce the phase noise accumulated on the timing signal along the synchronization chain while adding as little as possible internally generated clock phase noise, as to finally produce at its output a synchronization reference signal complying with the stability requirements recommended in [5].

In the case of a synchronization references loss, each node clock is required to autonomously generate, during the synchronization link restoring time, a timing signal suitable for synchronization of SDH equipment.

In order to achieve the above performance, it is necessary to design an advanced synchronization network, based on high performing timing devices, called SASE [6] (Stand Alone Synchronization Equipment), capable to receive, filter and distribute high quality timing references in each network node.

Telecom Italia started its activity in designing a new national synchronization network two years ago, following two main projects:

- development of a Master-Slave synchronization network, constituted by roughly 50 nodes, each of them provided with a SASE based on Rubidium (transit node) or quartz crystal (local node) oscillators, devoted to synchronize the long distance SDH transport network;
- development, both in the regional and in the access portion of the network, of a SASE based synch network suitable for synchronizing both SDH equipment and digital exchanges.

At present, the first project is under test in the field while the second one is in progress. For the correct design of the new

0-7803-2486-2/95 $4.00 © 1995 IEEE

national synchronization network it has been found essential to characterize timing performance of existing digital exchanges as well as the newly introduced SDH equipment and SASE units. Moreover, PDH links ability to transport timing references has been also checked.

In this paper, firstly the configuration measurement set-ups used in characterizing timing signal quality are introduced and discussed (sect.2); then the most important timing and synchronization standards established in regulatory bodies are identified (sect.3). Finally, the preliminary results obtained in the characterization of digital exchanges, SDH equipment, SASE units and PDH links are presented and analyzed, in order to provide useful inputs for the design of the new synchronization network (sect.4).

2. Stability quantities and measurement configurations

Several stability quantities able to characterize both clock and synchronization distribution network performance were proposed in standardization bodies [1-6] and in the scientific community [7,8]. Most of these quantities can be expressed in terms of the Time Error function TE(t) [9], that may be regarded as a measure of the error that the Clock Under Test (CUT) incurs in while trying to generate an ideal time scale t. As the ideal time scale is not available, the practical estimation of TE is performed using, as a reference clock, an actual clock considerably better performing than the CUT. In this case the effects of reference clock instabilities are negligible with respect to those of the CUT. Clock stability measurements are typically carried out based on methods which, using digital counters, allow to extract a sampled version of the function TE(t): the sequence of N values $TE_m=TE[t_0+(m-1)\tau_0]$, where t_0 is the initial observation time, τ_0 is the sampling period and $m=1, 2,...,N$, is used in order to estimate the most important stability quantities.

Two stability quantities are of particular interest in characterizing actual clocks [1-3], namely the Maximum Time Interval Error (MTIE) and the Time Deviation (TDEV). The most frequently used estimators of the MTIE and TDEV quantities are defined as follows

$$MTIE(\tau)= \max_{1\le k<N-n}\left[\max_{k\le i<k+n} TE_i - \min_{k\le i<k+n} TE_i\right], \quad n=1,2,\ldots,N-1$$

$$TDEV(\tau)= \left\{\frac{1}{6n^2(N-3n+1)}\cdot \sum_{i=1}^{N-3n+1}\left[\sum_{j=0}^{n-1}(TE_{j+2n+i}-2TE_{j+n+i}+TE_{j+i})\right]^2\right\}^{1/2}, \quad n=1,2,\ldots,\left\lfloor\frac{N}{3}\right\rfloor$$

where $\tau=n\tau_0$.

In characterizing actual clocks, two different TE measurement set-ups are of interest, as depicted in fig.1a and 1b. In the first set-up the timing signal from a Primary Clock (PC) (or from a free running Slave Clock (SC)) is compared with the timing signal at the output of a Measurement Reference Clock (MRC). In the second set-up, an SC is slaved to the output of the MRC. While the first configuration produces TE data reflecting all the instabilities due to both the MRC and the CUT, the second one produces TE data that reflect only the instabilities the SC adds to the reference timing signal [8,10]. Both measurements are essentially intended for in-lab assessment of autonomous or slave clock performance.

When measuring distributed timing signal quality across a synchronization network, two measurement configurations may be set-up, as shown in fig.2. Adopting the configuration shown in fig.2a, one gets TE data that are typically affected by two contributions, the first one accounting for relative time deviations between PRC and MRC (filtered by the clock chain), the second one resulting from internal SC instabilities accumulated along the clock chain. In some special cases, i.e., when the PRC is directly accessible to be used as MRC, it is possible to perform the measurement as depicted in fig.2b. In this second case, TE data are affected by SC instabilities accumulated along the chain only.

The four configurations depicted in figs.1 and 2 can be, in their turn, classified in two conceptually different categories.

Case 1

Independent Clock Configuration (see figs.1a and 2a): this case occurs when each one of the two clocks compared operates independently of the other; in order to get meaningful measurement results, the MRC must be sufficiently better performing than the CUT;

Case 2

Synchronized Clock Configuration (see figs.1b and 2b): this case occurs when the two clocks compared are part of a synchronization distribution network and are traceable to the same master clock.

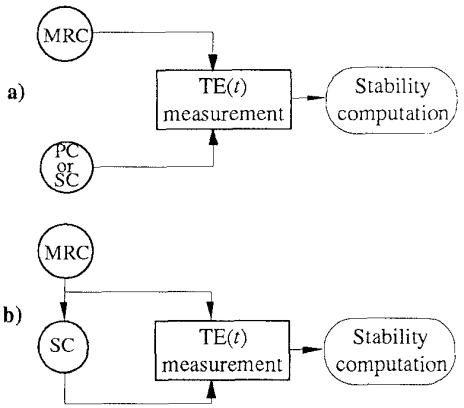
3. Standards for network synchronization

There are three important forums involved in the development of international standards or recommendations in the network synchronization field, namely ITU-T Study Group 13, ETSI TM-3 and ANSI T1.X1.

As far as the ITU-T is concerned, seven recommendations are relevant: rec.G.810 provides definitions concerning timing and synchronization issues; recs.G.811, G.812 and G.81s specify the timing requirements at the outputs of the synchronization network clocks; recs.G.823, G.824 and G.825 define the requirements for the control of jitter and wander within digital networks.

The ETSI DE/TM-3017 provides requirements for synchronization networks within the European Community. The standard deals with the definitions of a synchronization terminology (part 1), the synchronization network architecture (part 2), the control of jitter and wander within synchronization network (part 3) and the timing characteristics of network synchronization clocks (part 4, 5, and 6).

The ANSI T1-X1 Subcommittee produced the T1.101 standard which specifies synchronization interfaces for digital networks. This standard includes basic definitions, general outline of synchronization problems in digital networks, primary reference source specifications and reference interface specifications both for the optical interfaces OC-N (Optical Carrier level N) and the DS1 (Digital Signal level 1) interface.



MRC = Measurement Reference Clock ;
SC = Slave Clock; PC = Primary Clock

Fig.1 - Different configurations for clock stability measurements.

4. Measurement results

In this section, MTIE and TDEV measurement results, characterizing stability behaviour of timing signals at the output of digital exchanges, SDH equipment, SASE units and PDH links, are reported. All measurements were performed using the synchronized clock configuration, in order to identify the phase noise types [8] the SC adds to the reference signal.

In the case of equipment measurements (see fig.1b), the MRC adopted was a high quality Rubidium clock: the MRC provided a very stable reference timing signal (at 5 MHz) both to a high resolution time counter and to a signal generator used to synthetize the 2.048 MHz (or 2.048 Mbit/s) timing reference for the CUT. The phase of the timing signal at the output of the CUT was matched against the phase of the signal at its input by means of a computer assisted time counter. In such a way, a sequence of N time error samples equally time spaced, with a sampling period τ_0, was acquired, stored and subsequently used for calculating the stability quantities introduced in sect.2. From all the equipment measurement results presented here below (sect.4.1-3), and especially from the joint consideration of MTIE and TDEV behaviours, it is possible to recognize the presence of typical phase noise components and to highlight, for observation intervals greater than the inverse of the SC bandwidth B, both the SC filtering action on its own internal phase noise sources and the influence of the measurement configuration adopted [10].

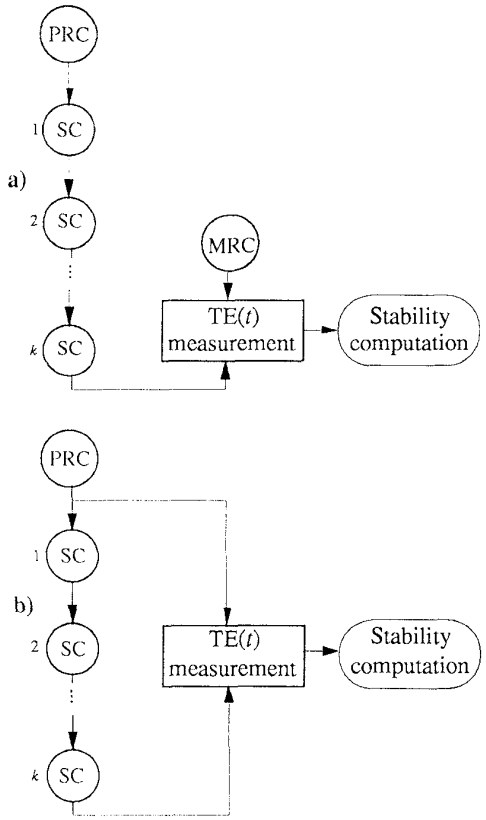
In the case of network measurements (see fig.2b), the MRC was a Cesium oscillator and the clock chain was constituted by two cascaded slave clocks, about 1000 km apart, being the transmission links based on PDH systems. The same measurement set-up as in the previous case was adopted.

4.1. Digital exchange timing units

For the characterization of timing performance of a digital exchange having bandwidth B=5 mHz a sequence of N=483,250 TE samples with sampling period τ_0=7.5 ms, corresponding to a total measurement observation time of about one hour, was taken. The results obtained for MTIE and TDEV quantities are shown in figs.5 and 6, respectively. Taking into account the properties of the stability quantities presented in [8], from the analysis figs.5 and 6 we can state that:

- the slopes of MTIE and TDEV for observation intervals up to 5 s reveal that a White Phase Modulation (WPM) noise is dominant [8];
- the slopes of MTIE and TDEV for observation intervals 10s<τ<200s reveal that a Flicker Frequency Modulation (FFM) noise is dominant [8].

The MTIE results for the digital exchange here considered are compliant with MTIE mask reported in rec.G.812.



MRC = Measurement Reference Clock ;
PRC = Primary Reference Clock ; SC = Slave Clock

Fig.2 - Different configurations for synchronization network stability measurements.

4.2. SDH equipment clock

As far as the characterization of timing performance of an SDH equipment (namely, an Add-Drop Multiplexer) clock is concerned, a sequence of N=267,000 TE samples with sampling period τ_0=7.5 ms, corresponding to a total measurement observation time of about half an hour, was acquired. The results obtained for MTIE and TDEV quantities are shown in figs.7 and 8, respectively. Analyzing figs.7 and 8 we can state that [8]:

- the slopes of TDEV for observation intervals up to 0.1 s reveal that a White Phase Modulation (WPM) is dominant [8];
- the slopes of TDEV for observation intervals 1s<τ<50s reveal that a Flicker Frequency Modulation (FFM) is dominant [8].

The MTIE results for the SDH equipment clock here considered are not compliant with constant temperature MTIE mask reported in Rec.G.81s, for observation intervals greater than 100 s.

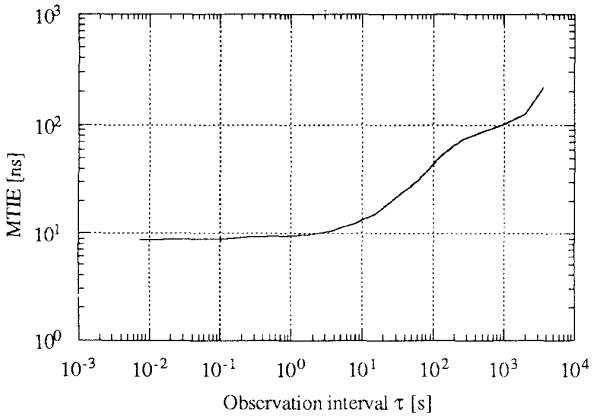


Fig.5 - MTIE experimental results for digital exchange timing unit.

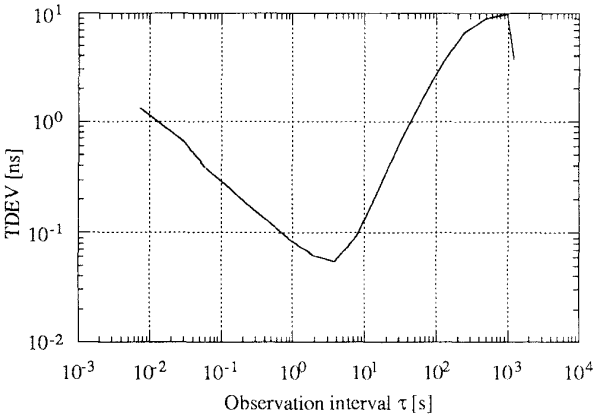


Fig.6 - TDEV experimental results for digital exchange timing unit.

4.3. SASE unit

As far as the characterization of timing performance of a SASE unit equipped with an internal OCXO (Oven Controlled Crystal Oscillator) is concerned, a sequence of N=483,250 TE samples with sampling period τ_0=7.5 ms, corresponding to a total measurement observation time of about one hour, was taken. The considered unit had a bandwidth B=10 mHz. The results obtained for MTIE and TDEV quantities are shown in figs.9 and 10, respectively. It has to be pointed out that for observation intervals up to 1 s the test-bed noise dominates: such a noise shows a WPM characteristic [8]. For observation intervals 1s<τ<50s figs.9 and 10 reveal that a Flicker Frequency Modulation (FFM) component is dominant [8].

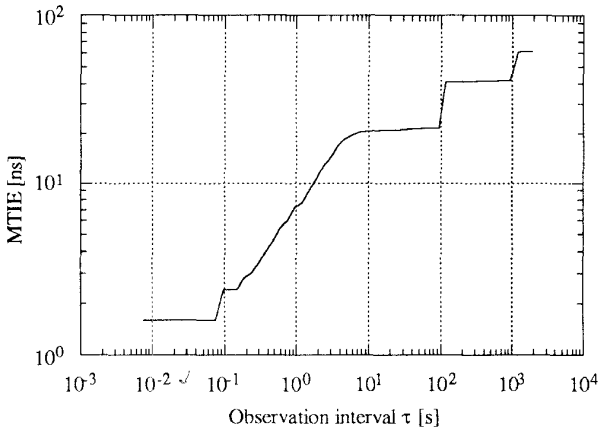


Fig.7 - MTIE experimental results for an SDH equipment.

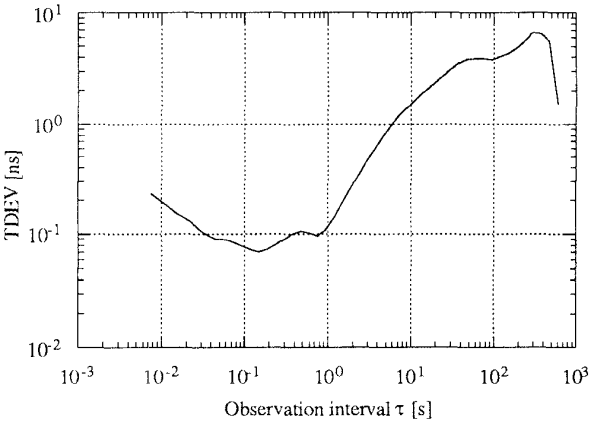


Fig.8 - TDEV experimental results for an SDH equipment.

4.4. TIMING PERFORMANCE OF A NETWORK BASED ON PDH LINKS

As far as the network measurement is concerned, a sequence of N=9500 TE samples with sampling period τ_0=750 ms, corresponding to a total measurement observation time of about two hours, was taken. The results obtained for MTIE and TDEV quantities are shown in figs.11 and 12, respectively. Analyzing these figures it is not possible to recognize unambiguously what type of phase noise is affecting the timing signal under measure. It is worthwhile to note that the phase noise level, as measured by means of the MTIE quantity, is as little as about 100 ns in all the observed time intervals .

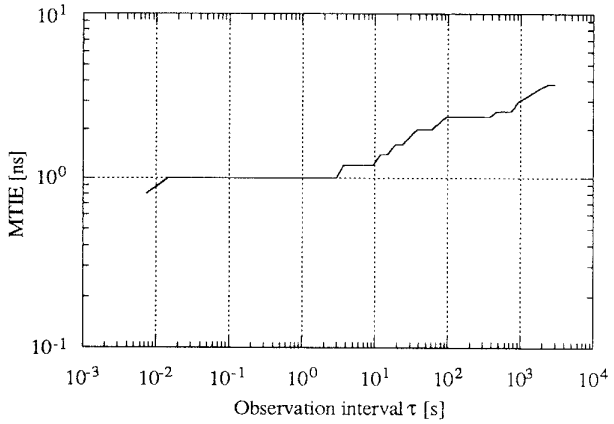


Fig.9 - MTIE experimental results for a SASE unit.

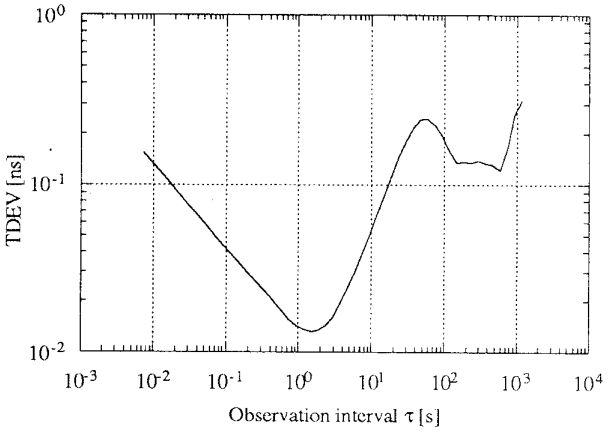


Fig.10 - TDEV experimental results for a SASE unit.

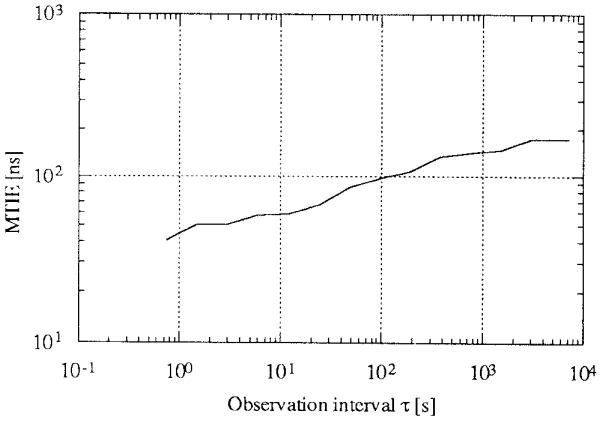


Fig.11 - MTIE experimental results for the network characterization.

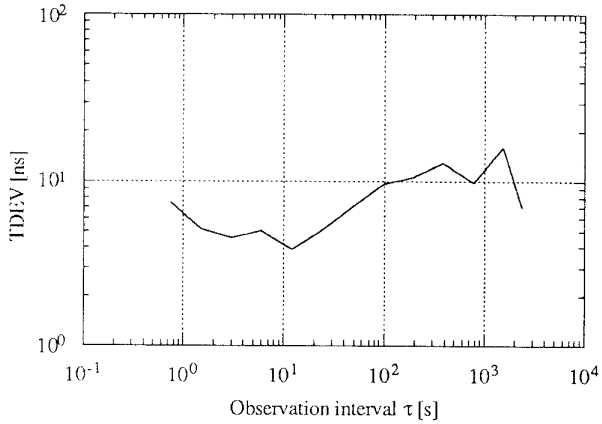


Fig.12 - TDEV experimental results for the network characterization.

5. Conclusions

The measurement results reported in this paper confirm the need for SASE units within an advanced synchronization network in order to guarantee high performance for the distributed timing signals. In fact, the digital exchange timing units, as well as SDH equipment clocks, generally show poor stability performance as compared to the requirements of synchronization networks; instead the excellent phase noise filtering capabilities together with the extremely low noise oscillator characteristics (MTIE less than 10 ns) provided by SASE units are essential for the provisioning of high quality timing references.

Moreover, it has been shown that the PDH links are suitable for the distribution, by means of 2.048 Mbit/s signals, of timing reference to network nodes where SDH interfaces are not available to be used for synchronization purposes.

Acknowledgement - The work of M. Carbonelli, D. De Seta and D. Perucchini was carried out in the framework of the agreement between the Italian PTT and the Fondazione Ugo Bordoni. This work was carried out while S. Bregni was with SIRTI.

REFERENCES

[1] ITU-T, Rec G.81s, Geneva, 1992.
[2] ITU-T, Rec. G.812, Blue book, vol.III, Melbourne, 1988.
[3] ITU-T, Rec. G.811, Blue book, vol.III, Melbourne, 1988.
[4] ITU-T, Rec. G.803, Blue book, vol.III, Melbourne, 1988.
[5] ITU-T, Rec. G.783, Blue book, vol.III, Geneva, 1992.
[6] ETSI, ETS DE/TM 3017, Montpellier, February 1994.
[7] D.W. Allan, *Time and frequency metrology: current status and future considerations*, 5° European Frequency and Time Forum, Besançon March 1991.
[8] M. Carbonelli, D. De Seta, D. Perucchini, *Clock stability measures for the assessment of synchronization network performance*, Proc. IEEE SICON ICIE '93, Singapore, September 1993, pp. 188-192.
[9] M. Carbonelli, D. De Seta, D. Perucchini, S. Ruffini, *Synchronization of SDH networks: slave clocks model and stability measures*, Proc IEEE GLOBECOM '92, Orlando, 6-9 December 1992, pp. 829-833.
[10] S. Bregni, M. Carbonelli, M. D'Agrosa, D. De Seta, D. Perucchini, *Different behaviour of frequency stability measures in independent and synchronized clocks: theoretical analysis and measurement results*, Proc. IEEE ICC '94, New Orleans, 1-5 May 1994, pp. 1066-1070.