Facing up to Practical Measurement of MRTIE: a New Effective Methodology

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Abstract

Maximum Relative Time Interval Error (MRTIE) is historically one of the main time domain quantities considered for the specification of clock stability requirements in telecommunications standards. In this work, after the formal definition of MRTIE, the main issue of its experimental measurement is pointed out: the heavy computational weight in most cases of practical interest. Therefore, an effective methodology, conceived with the aim of providing an easy - but accurate - way to test clocks compliance with MRTIE standard masks, is herein outlined and discussed. Moreover, several measurement results are provided. These results have been obtained throughout the last two years by testing clocks of widely deployed digital switching exchanges, clocks of commercial SDH equipment and state-of-the-art stand-alone slave clocks (SSUs) for synchronization networks.

1. Introduction

Synchronization plays a central role in digital telecommunications networks. Indeed, while transmission equipment designed for the Plesiochronous Digital Hierarchy (PDH) [1] does not need any network synchronization, since the multiplexing technique adopted allows - through bit justification - substantial frequency offsets between tributaries [2], digital switching equipment requires to be synchronized in order to avoid slips [3]. While slips do not heavily affect normal phone calls, they can even be catastrophic on some data services! The introduction of the circuit-switched data networks, and of new advanced services such as e.g. those provided by the emerging ISDN, yielded first to the need of more stringent synchronization requirements. As a matter of fact, however, the ongoing spreading of Synchronous Digital Hierarchy (SDH) [4] technology in telecommunications networks have really made synchronization a hot topic in Standard Bodies in the last few years: SDH heavily relies on network synchronization to meet all the claimed performance objectives.

As a consequence of SDH introduction, thus, completely new synchronization standards are presently being developed parallelly in ITU-T and ETSI, on the way led by ANSI. Current ITU-T Recs. G.810, G.811, G.812 [5], specifying primary and slave clocks suitable for PDH networks, will be thoroughly revised [6][7]. Moreover, a new Rec. G.81s [8] on SDH equipment clocks is under study, while a section of Rec. G.803 [9] deals with the SDH synchronization network architecture. On the European side, ETSI DE/TM-3017 [10] is by now under completion. A major topic of discussion in Standard Bodies is clock stability characterization. Among the quantities considered for the specification of stability requirements [6][10][11], *Maximum [Relative] Time Interval Error* (M[R]TIE) played historically a major role for characterizing timing interfaces in telecommunications networks (as it will be shown later, the bracketed [Relative] is optional, and denotes the measurement configuration). Unlike other frequency stability measures [12][13][14], all implying some kind of data averaging, MRTIE is a rough *peak* measure of the time deviation of a clock with respect to a known reference. This involves some delicate issues in accomplishing its practical measurement. In relevant standards, nevertheless, up to now no mention was made to easy, suitable test procedures to check clock compliance with MRTIE masks.

In a previous companion paper [15], some critical issues of MRTIE approach to SDH timing interfaces specification were outlined, and a measurement methodology was proposed and applied in order to provide more insight into the key features of this quantity. In this work, after the formal definition of MRTIE, the main issue of its experimental measurement is pointed out: the heavy computational weight in most cases of practical interest. Therefore, a suitable approach to face up to this issue is herein discussed. This proposed methodology was conceived with the aim of providing an easy - but accurate - way to test the compliance of telecommunications clocks with MRTIE standard masks. Thus, several measurement results are eventually provided. These results have been obtained throughout the last two years by testing clocks of widely deployed digital switching exchanges, clocks of commercial SDH equipment and state-of-the-art stand-alone slave clocks for synchronization networks.

2. What is MRTIE?

A general expression describing a pseudo-periodic waveform which models the timing signal $s(t)$ at the output of clocks is given by [12][13]

$$s(t) = A \sin \Phi(t) \tag{1}$$

where A is a constant amplitude coefficient and $\Phi(t)$ is the *total instantaneous phase*, expressing the ideal linear increasing with t and any frequency drift or random phase fluctuation.

The generated *Time* function $\mathrm{T}(t)$ of a clock is defined, in terms of its total instantaneous phase, as

$$\mathrm{T}(t) = \frac{\Phi(t)}{2\pi\nu_{\mathrm{nom}}} \tag{2}$$

where ν_{nom} represents the oscillator nominal frequency. It is worthwhile noticing that for an ideal clock $\mathrm{T}_{\mathrm{id}}(t)=t$ holds, as expected. For a given clock the *Time Error* function $\mathrm{TE}(t)$ (in standards also called $x(t)$) between its time $\mathrm{T}(t)$ and a reference time $\mathrm{T}_{\mathrm{ref}}(t)$, is defined as

$$x(t) \equiv \mathrm{TE}(t) = \mathrm{T}(t)-\mathrm{T}_{\mathrm{ref}}(t) \tag{3}$$

while the Time Error variation over an interval duration S is called *Time Interval Error* $\mathrm{TIE}_t(S)$ and is defined as

$$\mathrm{TIE}_t(S) = \mathrm{TE}(t+S)-\mathrm{TE}(t) \tag{4}$$

Finally, the *Maximum Time Interval Error* function $\mathrm{MTIE}_t(S)$ is defined as

$$\mathrm{MTIE}_t(S) = \max_{t\le\xi\le t+S} [\mathrm{TE}(\xi)] - \min_{t\le\xi\le t+S} [\mathrm{TE}(\xi)] \tag{5}$$

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and represents the maximum error committed by the clock under test in measuring a time interval over the whole interval $[t,t+S]$. Standard specifications [6][10][11] actually deal with MTIE(S,T), i.e. the maximum peak-to-peak deviation of TE in all possible observation intervals S within a measurement period T (see Fig. 1), defined as

$$\mathrm{MTIE}(S,T) = \max_{0 \le t \le T-S} \mathrm{MTIE}_t(S) \qquad (6)$$

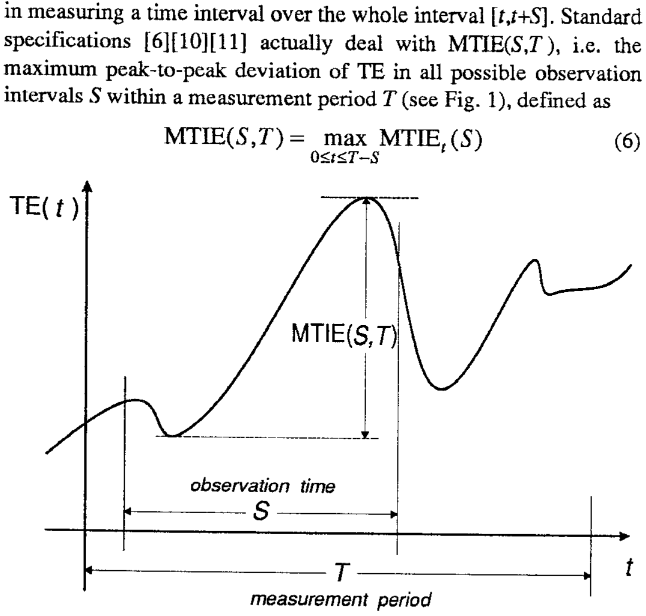

Fig. 1: Definition of MTIE(S,T)

MTIE(S,T) dependence on both the parameters S and T was discussed in [15]. The optional word *Relative* usually addresses the measurement set-up configuration: MTIE applies to the *independent clocks configuration*, MRTIE to the *synchronized clocks configuration* [6] [10][16]. In the former case, the reference time $T_{\mathrm{ref}}(t)$ of (3) is the absolute time t (in practice, it may be the time generated by a clock as a Primary Reference Clock [10]); in the latter, $T_{\mathrm{ref}}(t)$ is the input to a slave clock, while $T(t)$ is its output. This paper, for the sake of simplicity, is focused on MRTIE, but most considerations apply also to MTIE.

3. Measuring MRTIE

MRTIE measurement is usually based on the time domain measurement of the TE process $x(t)$ between the output of a slave Clock Under Test (CUT) and its input reference (see Fig. 2).

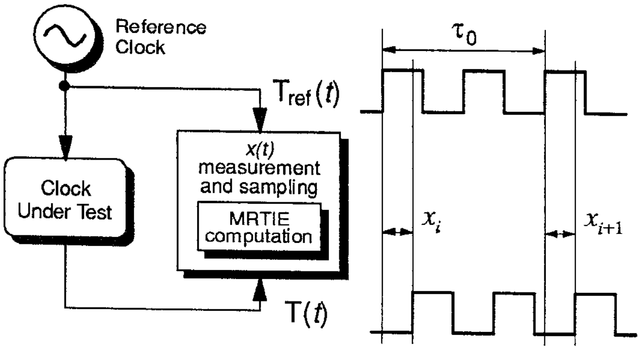

Fig. 2: Time Error measurement between the input and the output of a slave clock and MRTIE computation

Sequences of TE samples $\{x_i\}$, defined as

$$x_i = x\left(t_0 + (i-1)\tau_0\right) \qquad i = 1,2,3,\ldots \qquad (7)$$

where t_0 is the initial observation time and τ_0 is the sampling period, are measured using digital counters - and stored for numerical post-processing - over a total measurement period T. The samples x_i are typically measured between two corresponding zero-crossing of the timing signals at the input and the output of the CUT, as shown in Fig. 2.

3.1. Crude Computation

Starting from the TE measured sequence $\{x_i\}$, the most straightforward way to compute MRTIE(S,T) is to apply the formula (6) directly. Letting $N_T = T/\tau_0 + 1$ be the total number of available samples and $N_S = S/\tau_0 + 1$ be the number of samples available in the window of span S, to obtain a single value MRTIE(S,T) the following expression has to be computed

$$\mathrm{MRTIE}(S,T) = \max_{j=1}^{N_T-N_S+1}\left[\max_{i=j}^{N_S+j-1}(x_i) - \min_{i=j}^{N_S+j-1}(x_i)\right] \qquad (8)$$

MRTIE masks recently proposed in standards [8][10], still under discussion, span over a wide range of S: four decades, namely from 10^{-1} s up to 10^3 s. For a long time this range was even wider, from few milliseconds up to 10^5 s. Moreover, many researchers do agree not to consider MRTIE just a simple measure of wander, thus to be computed e.g. from sequences $\{x_i\}$ acquired with sampling period $\tau_0 \ge 0.1$ s and through a single-pole low-pass filter with cut-off frequency $f_{3\mathrm{dB}} = 10$ Hz, as suggested in [11]. Rather, MTIE(S,T) has proved very useful for characterizing clocks focusing on high frequency noise too; in this case, it should be computed on data collected at the highest possible rate, in order to capture the fastest phase fluctuations.

In our opinion, typical values of interest in characterizing a clock, also beyond mere conformance testing, are 1 ms $\le S \le$ 1000 s and T in the order of few hours or more, while the target sampling period would be $\tau_0 = 488$ ns for a 2.048 MHz timing signal. It obviously appears that the direct computation of the estimator (8) easily tends to be unmanageable, as in the suggested example $2048 \le N_S \le 2 \cdot 10^9$ and $N_T \cong 10^{10}$-10^{11}!

3.2. Suitable Approaches to Practical Measurement

Different approaches can be envisaged to face up to the issue of storing and processing this huge amount of data, and therefore to accomplish the practical measurement of MRTIE without having a supercomputer.

A first approach is to contrive a suitable efficient algorithm alternative to the crude evaluation of (8). Any computational trick (except real-time data processing), however, would not let us avoid storing all those data.

A second one, which is up to now most widely applied in synchronization interfaces testing, consists - trivial but effective - in drastically reducing the number N_T of samples x_i to process. This is achievable through shortening the measurement period T and/or lengthening the sampling period τ_0 (equivalent to samples decimation). As an example, it is worthwhile noticing that, referring to the case suggested at the end of section 3.1, achieving N_T in the order of 10^5 is possible by letting e.g. $T = 50$ ms, $\tau_0 = 488$ ns (if aiming at exploiting the maximum sampling rate) or $T = 24$ h, $\tau_0 = 860$ ms (if aiming at observing the clock over a long measurement period).

A third approach, completely alternative, is outlined in the next section. This methodology was conceived with the aim of providing an easy way to test the compliance of telecommunications clocks with MRTIE standard masks, without giving up the maximum achievable sampling rate of $x(t)$.

4. Proposed Methodology: MRTIE Measurement on Disjointed Intervals

The underlying idea is not to consider *all* the sliding windows of width S over the measurement period, but to perform a sequence of M consecutive independent measurements of MRTIE(S), as shown in Fig. 3, each one taking into account disjointed sets of samples x_i collected at the maximum rate allowed by the measurement instrument.

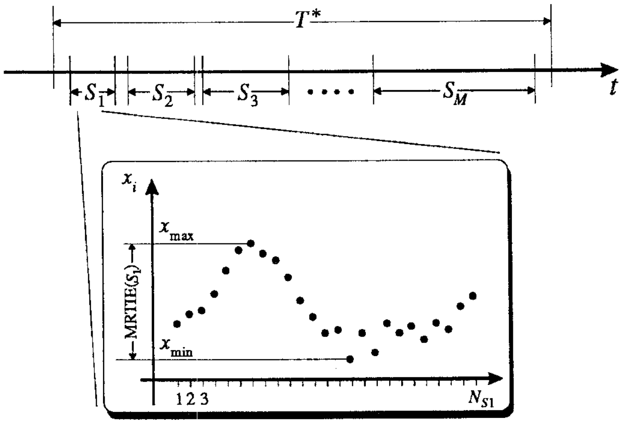

Fig. 3: MRTIE(S) measurement on disjointed intervals

Each MRTIE(S) measurement is done by letting T=S in (8). Thus

$$\mathrm{MRTIE}(S) = \max_{i=1}^{N_S}(x_i) - \min_{i=1}^{N_S}(x_i) \qquad (9)$$

In Fig. 3, the measurement period was marked with T^*, since it has nothing to do with T of Fig. 1 and (8): here it is simply the period during which the clock was under test including dead time between measurements. Moreover, M different measurements MRTIE(S) can be accomplished in sequence varying S step by step from a minimum value S_{MIN} up to a maximum S_{MAX} as a geometric progression of ratio

$$\rho = \sqrt[M-1]{\frac{S_{MAX}}{S_{MIN}}} \qquad (10)$$

The spirit is to collect M snapshots of the clock peak-to-peak noise, by evenly sweeping the interval of interest $[S_{MIN}, S_{MAX}]$. Since the expression (9) is very simple, it can be evaluated in real time (e.g. in hardware) with virtually no limits on the number of samples x_i to process, thus allowing to achieve the maximum sampling rate without worrying about data storage and, what's more, the time needed to compute (8). The output of this test procedure is a scatter diagram typically showing a cloud of points (measurement results) of coordinates S, MRTIE(S), which represent the CUT behaviour during the whole measurement period T^*. *Necessary condition* for the clock compliance with standards is that *all* the measured points be below the specified mask. Obviously, the test is as stricter as bigger is the number M of successive MRTIE measurements.

5. Measurement Results

The methodology outlined has been extensively applied throughout the last two years in testing several timing devices, for conformance testing and to research purposes. The MRTIE measurement test bench, according to the diagram of principle in Fig. 2, is outlined in Fig. 4. A high performance time counter, with a resolution of 200 ps, measures the Time Error $x(t)$ between the output timing signal of the CUT and its input reference, synthesized from a rubidium frequency standard which also supplies the time base to the time counter. Both timing signals are 2.048 MHz sine waves.

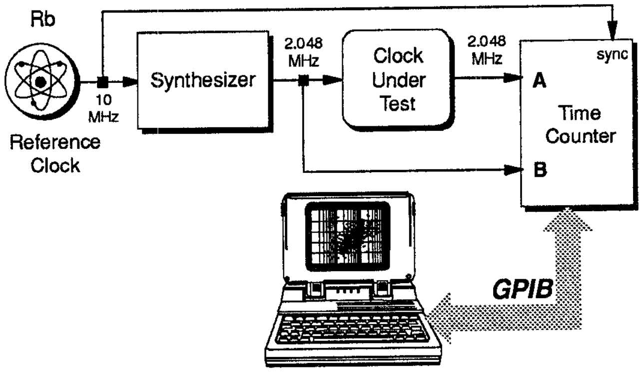

Fig. 4: MRTIE measurement test bench

The time counter is driven via a GPIB IEEE488.2 interface by a personal computer, which manages the sequence of M successive MRTIE(S) measurements setting increasing values of S as the geometric progression of ratio ρ (10). A special hardware function of the time counter allows real-time evaluation of (9) on up to $2 \cdot 10^9$ TE samples x_i measured on *every* timing signal edge, i.e. at the maximum sampling rate of 2.048 MHz (τ_0=488 ns).

Herein, some measurement results are provided. These results were obtained by testing the clocks of two widely deployed digital switching exchanges (suppliers A, B), the clocks of three commercial SDH equipment (suppliers C, D) and two state-of-the-art stand-alone slave clocks for synchronization networks (suppliers E, F). With standard terminology, we refer to SDH equipment clocks as *Synchronous Equipment Clocks* (SECs), while to stand-alone slave clocks as *Synchronization Supply Units* (SSUs). The SDH equipment under test was a Line Terminal Multiplexer STM-16 (LT-16) and three Add-Drop Multiplexers STM-1 (ADM-1) and STM-4 (ADM-4). Measurement results are shown in Figs. from 5 to 12. For easier understanding, the actual values of parameters S_{MIN}, S_{MAX}, M, T^* for each test - together with the CUT type - are summarized in Tab. 1, since tests were not accomplished in the same campaign.

Fig.	CUT Type	S_{MIN}	S_{MAX}	M	T^*
5	digital switch A clock (OCXO[1])	1 ms	500 s	200	~2.5 h
6	digital switch B clock (OCXO[1])	1 ms	100 s	100	~15'
7	LT-16 SEC C (TCXO[2])	1 ms	1000 s	100	~2.5 h
8	ADM-1 SEC C (TCXO[2])	1 ms	1000 s	100	~2.5 h
9	ADM-1 SEC D (TCXO[2])	1 ms	500 s	300	~3.5 h
10	ADM-4 SEC D (TCXO[2])	1 ms	1000 s	500	~10.5 h
11	SSU E (OCXO[1])	1 ms	1000 s	1000	~21 h
12	SSU F (OCXO[1])	1 ms	1000 s	100	~2.5 h

[1] *Oven Controlled Crystal Oscillator (quartz)*
[2] *Temperature Compensated Crystal Oscillator (quartz)*

Tab. 1: Actual measurement parameters for the results shown

MRTIE graphs regarding SECs (Figs. from 7 to 10) depict also the limits specified in relevant standards: the MRTIE mask specified in the latest draft version of [8] and part 5 of [10] is the solid line G.81s-2, while the old mask, for a very long time in force, specified in the previous versions is the dashed line G.81s-1.

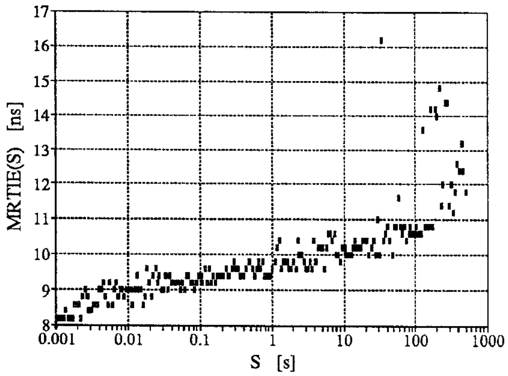

Fig. 5: MRTIE values measured on the clock of the digital switch A

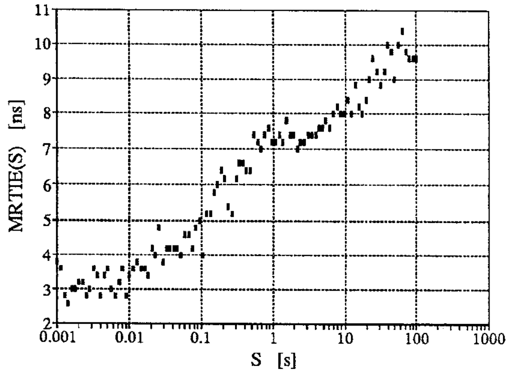

Fig. 6: MRTIE values measured on the clock of the digital switch B

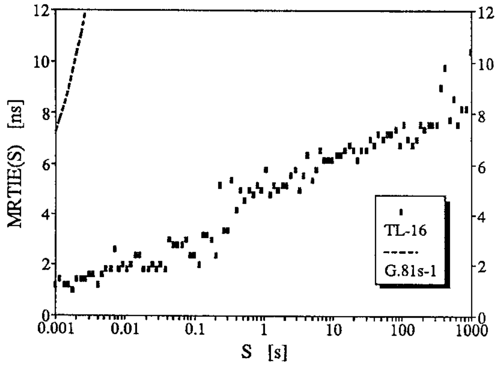

Fig. 7: MRTIE values measured on the SEC of a LT-16 (supplier C) vs. G.81s mask

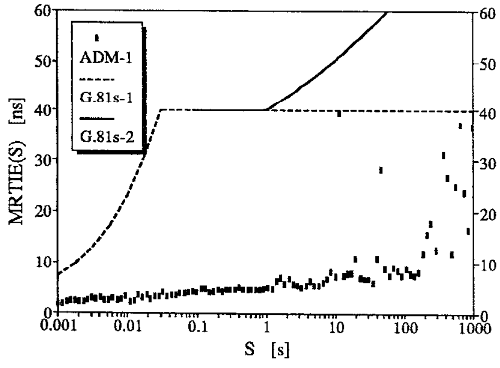

Fig. 8: MRTIE values measured on the SEC of an ADM-1 (supplier C) vs. G.81s mask

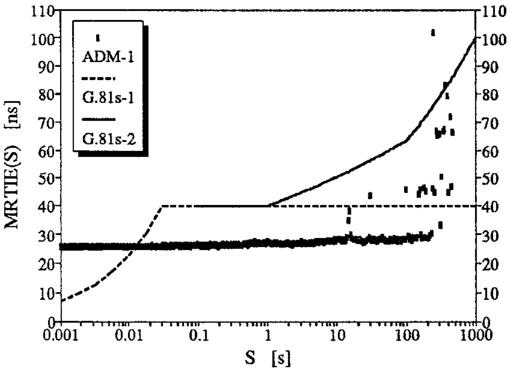

Fig. 9: MRTIE values measured on the SEC of an ADM-1 (supplier D) vs. G.81s mask

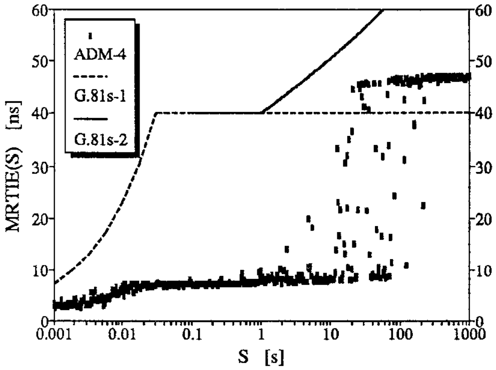

Fig. 10: MRTIE values measured on the SEC of an ADM-4 (supplier D) vs. G.81s mask

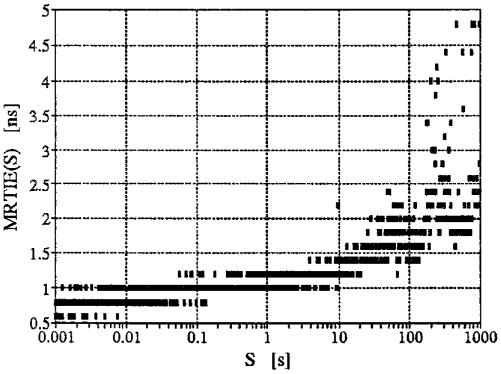

Fig. 11: MRTIE values measured on a SSU (supplier E)

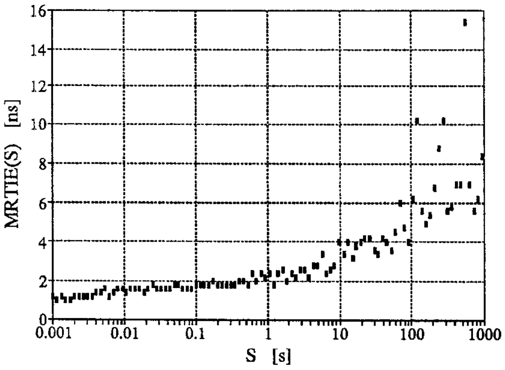

Fig. 12: MRTIE(*S*) values measured on a SSU (supplier F)

As shown by the graphs provided, some SECs exhibit higher noise (see Figs. 8, 9, 10) than other CUTs, as implemented with lower cost oscillators. The ADM-1 SEC in Fig. 9, in particular, even is not compliant with the original mask G.81s-1, since it exhibits a 26 ns noise floor also for $S \leq 13$ ms, and besides some measured MRTIE values are above the limits in the range $10\ \text{s} \leq S \leq 1000\ \text{s}$. The new mask G.81s-2, on the contrary, is much more permissive, so that almost all the measured values are below those limits. Analogous considerations apply for the SEC of ADM-4 in Fig. 10: while the measured values for $S > 10$ s are well over the original mask G.81s-1, the new mask G.81s-2 has granted "amnesty", allowing under the limits also the 46 ns values (it is worthwhile noticing that both these SECs are made by the same supplier, and that the SEC of ADM-4 should be an improved version of the former). Nevertheless, while measurements on SSUs were accomplished in laboratory and those on digital exchanges clocks in a test plant, thus in controlled conditions (e.g. with constant temperature), measurements on SECs were carried out on equipment deployed, for a SDH field trial, in an in-service telephone office. Not surprisingly, the clock featuring the best performance is a SSU (Fig. 11). Such clocks are designed to distribute their timing signal to other SSUs of the synchronization network and to all the equipment in their office, and therefore they offer the highest precision and stability. Moreover, we want to draw the reader's attention to some important considerations concerning all the graphs shown.

- Clocks are complex machines, mostly Digital Phase-Locked Loops (DPLL) [17], with control electronics (e.g. microprocessors) around the oscillator basic core. Hence, the output noise may be considerably bigger - and with a different spectrum - than that generated just by the internal oscillator.
- Values of MRTIE(S), measured according to the proposed methodology, always exhibit an *average* increasing trend with S, since by broadening the observation time S it is more likely to capture higher noise peaks. Moreover, increasing S allows to detect slower phase changes, i.e. with most part of the power spectrum gathered at the lowest frequencies (i.e. as $1/f^{\alpha}$ with α=1,2,3,4 [12][13]).
- According to our tests (not shown in this paper), measurements accomplished in conformity with the proposed methodology yield to slightly worse results (i.e. to higher MRTIE(S) values being equal S), compared to those obtained through the usual approach, outlined in sec. 3.2, of evaluating the estimator (8) on *short* sequences $\{x_i\}$ as sampled at a much lower rate. This is quite natural, since the peak-to-peak deviation of a set of N_S TE samples, spanning an observation interval S, is greater for larger N_S (keeping constant S, i.e. by decreasing τ_0): thinking to a gaussian noise model, collecting more samples the histogram tails stretch out! We remind, once again, that in the graphs shown MRTIE(S=1000 s) measurements consider $2 \cdot 10^9$ samples.

Finally, we point out that the proposed methodology distinguishes itself for its ability in capturing the fastest phase fluctuations, thus allowing very little values of S in characterizing clocks with MRTIE. Moreover, scatter diagrams are very useful in rendering the statistics of measured values: clouds thicken where values are more likely.

6. Conclusions

In this work, a new measurement methodology, providing an easy but accurate way to test clocks compliance with MRTIE standard masks, was outlined. Moreover, several measurement results were provided. These results have been obtained throughout the last two years by testing clocks of widely deployed digital switches, SECs and SSUs. The proposed methodology has proved to be effective and very useful, both for strict conformance testing of clocks and for gaining more insight into actual performance of commercial timing equipment in terms of peak-to-peak phase noise.

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