Timing Rearrangements of SEC and SASE Slave Clock Chains Due to Non-Small Input Phase and Frequency Hits in Synchronization Networks

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***Abstract* — In synchronization networks, chains of slave clocks (viz. SASE, SEC) transfer timing along synchronization trails. Hence, the need to assess precisely the performance of timing transfer along such chains, not only in stationary conditions, but also under transient rearrangements occurring after phase and frequency hits on the timing reference. In this work, the non-linear transient behavior of SEC and SASE clock chains has been simulated in the time domain, in order to evaluate their timing rearrangements after non-small phase and frequency hits on the reference. Both homogeneous and non-homogeneous chains of SEC and SASE clocks have been studied in various configurations, in order to provide synchronization engineers with a comprehensive survey, both in qualitative and quantitative terms, on the timing performance achievable when planning synchronization trails of various type and length.**

***Index Terms* — Clocks, phase-locked loops, SONET, synchronous digital hierarchy, synchronization of digital networks.**

I. Introduction

Network synchronization has gained increasing importance in telecommunications throughout the last 30 years [1]-[3]. Actually, the quality of most services offered by network operators is affected by network synchronization performance. The synchronization network is the facility implementing network synchronization. It provides all networks served with reference timing signals of required quality. Most modern operators have set up one or more synchronization networks to synchronize their switching and transmission networks, beginning with SDH/SONET backbone facilities.

Basic elements of synchronization network are nodes (autonomous and slave clocks) and links interconnecting them (e.g., 2 Mbit/s transmission facilities). An *autonomous clock* is a stand-alone device able to generate a timing signal, starting from some periodic physical phenomenon. A *slave clock*, on the other hand, is a device able to generate a timing signal having phase (or much less frequently frequency) controlled by a reference timing signal at its input. Slave clocks are usually based on Phase-Locked Loop (PLL) schemes [4].

In the synchronization network standard architecture defined by ITU-T and ETSI [5][6], based on the Hierarchical Master-Slave (HMS) strategy, the network master autonomous clock is called *Primary Reference Clock* (PRC). Moreover, in very short, two types of slave clock are defined: the building clock synchronizing all equipment within an office building, called *Synchronization Supply Unit* (SSU) or *Stand-Alone Synchronization Equipment* (SASE), and the *SDH Equipment Clock* (SEC).

In synchronization networks, chains of SEC and SASE slave clocks are the basic systems to transfer timing along *synchronization trails*. Since the introduction of SDH/SONET and of advanced digital services, clocks have been required to comply with stringent requirements by international standards [6]—[10]. Hence, the need to assess precisely timing transfer performance along such chains of slave clocks, not only in stationary conditions, but also under transient rearrangements occurring for example after reference switching.

Rather surprisingly, especially if compared to the huge literature available on PLL theory, in very few works chains of slave clocks have been analyzed. In paper [11], slave clock chains were studied under the simple hypothesis of linear behavior, deriving some indicative results on the accumulation of small-amplitude phase random noise along synchronization trails. Moreover, in paper [12], random noise accumulation in slave clock chains was studied by a time-domain state-space approach and by considering both linear and non-linear PLL models with additive noise sources. Nevertheless, not much attention has been devoted in literature to investigate important issues for the synchronization planner, such as evaluating the transient response of clock chains to non-small reference impairments, both in qualitative and quantitative terms, in particular depending on the type and number of standard chained clocks.

Therefore, in this work, the non-linear transient behavior of SASE and SEC slave clock chains has been simulated in the time domain, in order to evaluate their timing rearrangements after non-small phase and frequency hits on the reference signal. An example of practical case in which a slave clock experiences a phase step on the input may be when it switches reference between two network signals, both traceable to the same master clock. On the other hand, a frequency step is experienced when the slave clock switches reference between two plesiochronous timing signals, i.e. two signals traceable to independent clocks with same nominal frequency.

In this paper, a homogeneous chain made of 20 SECs is first studied, evaluating its response to input phase and frequency steps of various amplitudes and for different values of clock damping ratio. Then, homogeneous chains of 1 to 40 SECs are studied versus chain length. Finally, non-homogeneous chains

made of a variable number of SEC and SASE clocks are also considered, in order to provide synchronization engineers with a comprehensive survey on the timing performance achievable when planning synchronization trails of various type and length.

II. ITU-T and ETSI Synchronization Reference Chain

Modern synchronization networks are mostly based on the HMS architecture, recommended by international standards [5][6] and organized hierarchically in levels. Timing is distributed from the PRC down to all other nodes, along chains of SSU/SASE slave clocks in tandem connection. Moreover, timing can be transferred between SSU/SASE clocks along chains of SECs. The following basic features distinguish PRC, SSU/SASE and SEC clocks:

- the PRC runs autonomously and has the highest frequency accuracy and stability (cf. ITU-T Rec. G.811 [8]);
- the SSU/SASE is a slave clock synchronizing all other clocks in the office building and other "son" nodes in the HMS architecture; its loop time constant is thus very long (typically, at least 1000 s), to filter out as much timing impairments as possible (cf. ITU-T Rec. G.812 [9]);
- the SEC is a slave clock with poor long-term stability requirements and short loop time constant (typically, not above 1 s) (cf. ITU-T Rec. G.813 [10]).

Thus, chains of SEC and SASE slave clocks transfer timing along synchronization trails. ITU-T and ETSI defined the standard *reference chain* shown in Fig. 1. The first clock in the chain is the PRC. From it, a chain of slave node clocks (SSU/SASE) is built: intermediate SSUs are called transit-node SSUs, the last one may be a transit- or a local-node SSU. SSUs are linked via a variable number of SECs.

To meet synchronization requirements, the longest chain is recommended to not exceed M SSUs with up to N SECs interconnecting any two SSUs, where the values for the worst-case synchronization reference chain are M=10 and N=20, with total number of SECs limited to 60. In practical design, the number of chained clocks should be minimized for reliability and performance reasons. In this work, we studied also longer chains, in order to provide synchronization network planners with a wider set of performance data.

III. System Model

A. Model of Slave Clock

We considered slave clocks based on an analog PLL scheme with ideal-multiplier phase detector, where the input and output signals [V] are respectively given by

$$\begin{aligned} s_{\text{in}}(t) &= \sin[\omega_0 t + \theta_{\text{in}}(t)] \\ s_{\text{out}}(t) &= \sin[\omega_0 t + \theta_{\text{out}}(t)] \end{aligned} \qquad (1)$$

with the phase deviations $\theta_{\text{in}}(t)$ and $\theta_{\text{out}}(t)$ [rad] slowly varying with respect to ω_0 [rad/s]. Any difference in instantaneous frequency among the two signals is included in $\theta_{\text{out}}(t)$, as

$$\omega_{\text{out}}(t) = \omega_0 + \frac{d\theta_{\text{out}}(t)}{dt} \qquad (2).$$

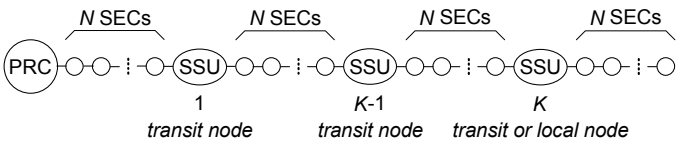

Fig. 1: ITU-T and ETSI synchronization network reference chain [5][6].

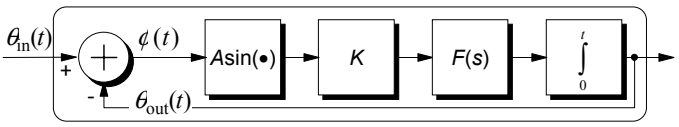

Fig. 2: Baseband model of PLL with ideal-multiplier phase detector.

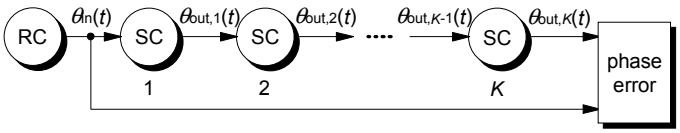

Fig. 3: Baseband model of chain of slave clocks with phase error measurement in synchronized-clock configuration.

We assumed the baseband equivalent model of PLL represented in Fig. 2, obeying the following dynamic equation [4] for the phase error $\phi(t)=\theta_{\text{in}}(t)-\theta_{\text{out}}(t)$

$$\frac{d\phi(t)}{dt} = \frac{d\theta_{\text{in}}(t)}{dt} - KA\int_0^t f(t-u)\sin\phi(u)\,du \qquad (3)$$

where the product KA [$s^{-1}V^{-1}$] is called loop gain and $f(t)$ is the impulse response of the loop filter with transfer function $F(s)$. This is a *baseband* model of the PLL, because centered on the phase error $\phi(t)$ independently of the quiescent frequency ω_0. Moreover, it is a *non-linear* model, due to the sin() function that makes arduous its mathematical analysis.

The transient response of the system for any input signal can be evaluated in the time domain by solving the dynamic equation (3), which in most cases can be done only by numerical computation.

B. Model of Slave Clock Chain

The baseband model of slave clock chain studied in this paper is shown in Fig. 3. A chain of K slave clocks is considered and the synchronized-clock configuration [7] for relative phase error measurement is adopted: the timing signal output by the K-th Slave Clock (SC) of the chain is compared to the input reference from a Reference Clock (RC).

Consistently with the slave clock model defined in the previous section, let the timing signal at the input of the chain be affected by a given phase deviation $\theta_{\text{in}}(t)$ [rad]. On the other hand, the phase at the output of the j-th clock of the chain is denoted with $\theta_{\text{out},j}(t)$ [rad] (for j=1, 2, ..., K). Analogously, angular frequency deviations at the input and output of the chain are denoted with $\Delta\omega_{\text{in}}(t)$ and $\Delta\omega_{\text{out}}(t)$.

C. Model of SASE

According to standard specifications [9] and to most practical realizations available on the market, the SASE model adopted in all simulations of this work is a second-order

type-2 PLL, with active loop filter having transfer function $F(s)=(1+sT_2)/sT_1$ arranged to get closed-loop bandwidth (i.e., -3-dB cut-off frequency) B=1 mHz and damping ratio $\zeta\geq 3$.

We remind that, in a second-order PLL, bandwidth B, damping ratio ζ and natural frequency ω_n are related by

$$B=\frac{\omega_n}{2\pi}\sqrt{2\zeta^2+1+\sqrt{\left(2\zeta^2+1\right)^2+1}} \qquad (4).$$

D. Model of SEC

According to standard specifications [10], and to most practical realizations available on the market, the SEC model adopted in all simulations of this work is a second-order type-2 PLL, with active loop filter having transfer function $F(s)=(1+sT_2)/sT_1$ arranged to have closed-loop bandwidth B=1 Hz and damping ratio $\zeta\geq 3$.

IV. Simulation Results: Homogeneous Chains of SECs

A. Chain of N=20 SECs

A homogeneous chain of N=20 SECs (B=1 Hz, ζ=4, $\omega_n\cong 0.77$ rad/s), i.e. the longest SEC chain in the standard reference chain (cf. Fig. 1), is considered. The time-domain responses to input phase steps starting at t=5 s and of amplitude $\theta_{in}=\pi/4$, $\pi/2$, $(3/4)\pi$, $(1\text{-}10^{-8})\pi$ are shown in graphs of Fig. 4, which plot the output phase $\theta_{out,20}(t)$ and the phase error $\phi_{20}(t)=\theta_{in}(t)-\theta_{out,20}(t)$ respectively, compared to input steps.

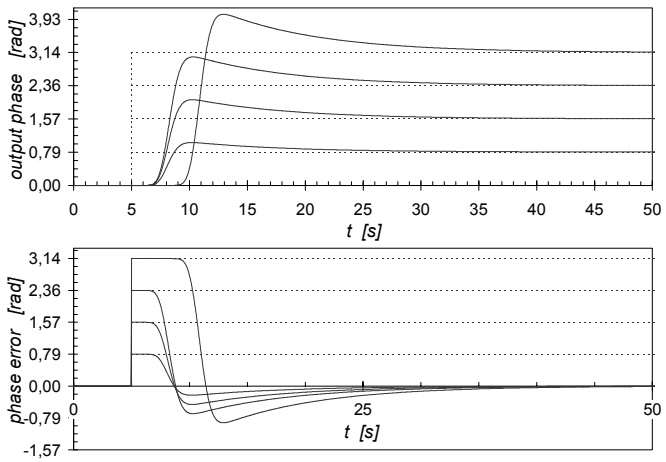

Fig. 4: Output phase and phase error of a chain of N=20 SECs (B=1 Hz, ζ=4) due to input phase steps $\theta_{in}=\pi/4$, $\pi/2$, $(3/4)\pi$, $(1\text{-}10^{-8})\pi$.

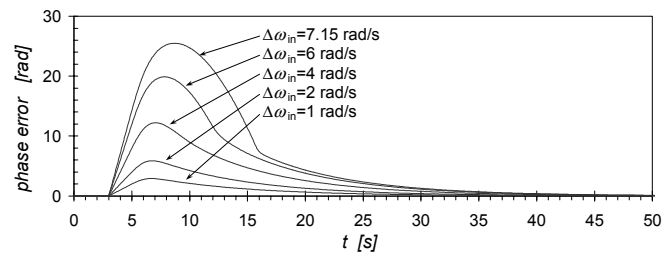

Fig. 5: Phase error of a chain of N=20 SECs (B=1 Hz, ζ=4) due to input frequency steps $\Delta\omega_{in}$=1, 2, 4, 6, 7.15 rad/s.

By inspection of these graphs, note first the very slow attack of transient responses: a chain of 20 second-order PLLs makes up a system with 40 poles and 20 zeroes and thus the first 19 derivatives of $\theta_{out,20}(t)$ in t=5 s are null. Note also the even slower response to the $(1\text{-}10^{-8})\pi$ phase step: the system dwells near $\phi_{20}(t)=\pi$ because that is unstable equilibrium point (system *hang-up* [4][13]).

Similarly, the responses to frequency steps starting at t=3 s and of amplitude $\Delta\omega_{in}$=1, 2, 4, 6, 7.15 rad/s at the input are shown in Fig. 5, which plots the phase error $\phi_{20}(t)$. On this graph, note that phase-relocking gets more arduous and the PLL behavior departs significantly from the linear model as the input step approaches the PLL pull-out frequency [4], which in this case can be evaluated $\Delta\omega_{po}\cong 7.24$ rad/s.

B. SEC Chains of Variable Length N

Variable-length homogeneous chains of N SECs (B=1 Hz, ζ=4, $\omega_n\cong 0.77$ rad/s) have been studied, for N=1, 5, 10, 15, 20, 25, 30, 35, 40. Their response to an input phase step starting at t=1 s and of amplitude $\theta_{in}=(3/4)\pi$ is shown in graphs of Fig. 6, which plot the output phase $\theta_{out,N}(t)$ and the phase error $\phi_N(t)$, respectively, compared to the input step.

Moreover, Fig. 7 plots some common descriptive measures of the transient responses so evaluated [4]: the *rise time* T_r, i.e. the time needed for the response to reach the input step amplitude, the *settling time* T_s, i.e. the time needed for the response to settle within an error not higher than ±5% around the input step amplitude, and the *peak overshoot* M_p, i.e. the maximum deviation of the response from the input step amplitude, expressed as percentage of it. By inspection, note that the settling time increases less than linearly with N, while the rise time and the peak overshoot exhibit almost exact linear dependence on it in the full range $1\leq N\leq 40$.

Similarly, the response of the chains to an input frequency step starting at t=5 s and of amplitude $\Delta\omega_{in}$=6 rad/s is shown in Fig. 8, which plots the phase error $\phi_N(t)$. Moreover, Fig. 9 plots the settling time T_s (which in this case we redefined conventionally as the time needed for the response to approach the input phase ramp within an error ≤1 rad) and the peak phase error *PPE*. There, note that the transient gets more arduous as longer is the chain. Furthermore, the settling time so defined depends less than linearly on N (it even does not increase for N>20), while the PPE exhibits linear dependence on N.

C. Chain of N=20 SECs with Variable Damping Ratio ζ

A homogeneous chain of N=20 SECs (B=1 Hz), with variable damping ratio ζ=3, 3.5, 4, 5, 7 (corresponding to $\omega_n\cong 1\div 0.45$ rad/s), is considered. Its response to an input phase step starting at t=1 s and of amplitude $\theta_{in}=(3/4)\pi$ is shown in graphs of Fig. 10, which plot the output phase $\theta_{out,20}(t)$ and the phase error $\phi_{20}(t)$, respectively, compared to the input step. Moreover, Fig. 11 plots the rise time T_r, the settling time T_s and the peak overshoot M_p. Not surprisingly, the damping ratio affects both the peak overshoot and the settling time of the chain, as it happens to a single clock.

Similarly, the response of the chain to an input frequency step starting at t=5 s and of amplitude $\Delta\omega_{in}$=6 rad/s is shown in Fig. 12, which plots the phase error $\phi_{20}(t)$. Moreover, Fig. 13 plots the settling time T_s and the peak phase error *PPE* (both defined as for Fig. 9). Here, note that the damping ratio does affect the settling time, but not the peak phase error.

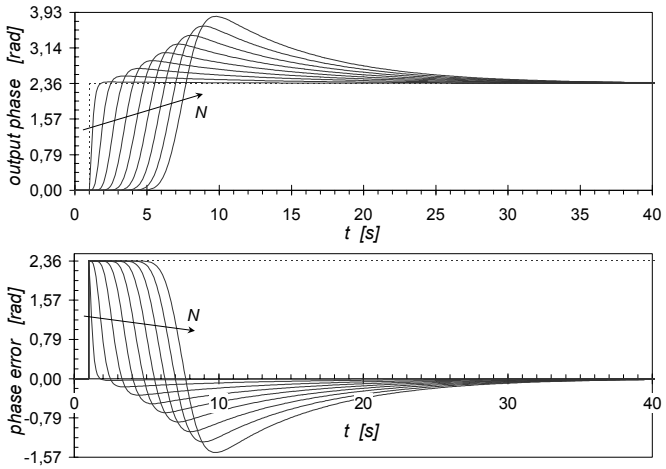

Fig. 6: Output phase and phase error of chains of N SECs (B=1 Hz, ζ=4) for N=1, 5, 10, 15, 20, 25, 30, 35, 40 due to an input phase step $\theta_{in}=(3/4)\pi$.

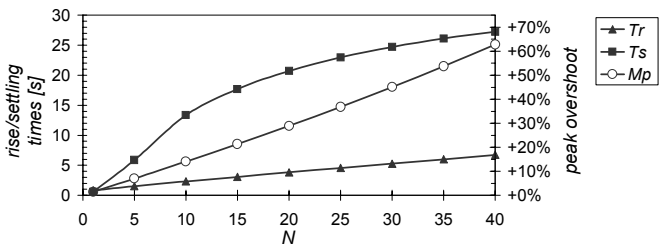

Fig. 7: Rise time T_r, settling time T_s and peak overshoot M_p of the output phase of chains of N SECs (B=1 Hz, ζ=4, input phase step $\theta_{in}=(3/4)\pi$).

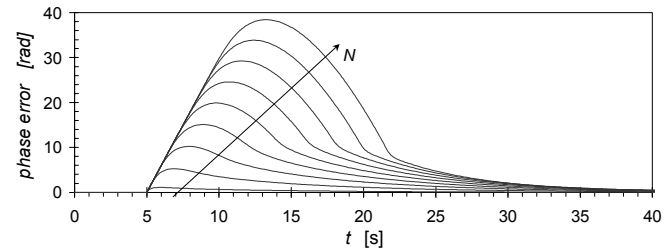

Fig. 8: Phase error of chains of N SECs (B=1 Hz, ζ=4) for N=1, 5, 10, 15, 20, 25, 30, 35, 40 due to an input frequency step $\Delta\omega_{in}$=6 rad/s.

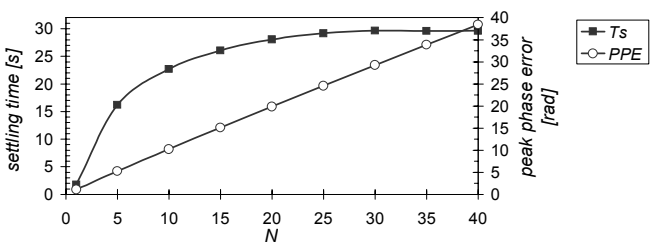

Fig. 9: Settling time T_s and peak phase error *PPE* of the output of chains of N SECs (B=1 Hz, ζ=4, input frequency step $\Delta\omega_{in}$=6 rad/s).

V. Simulation Results: Non-Homogeneous Chains of SEC and SASE Clocks

In this section, non-homogeneous chains made by cascading M+1 subchains, each made of N SECs and with one SASE clock between each subchain and the next one as in Fig. 1 (M SASE clocks in total), are considered.

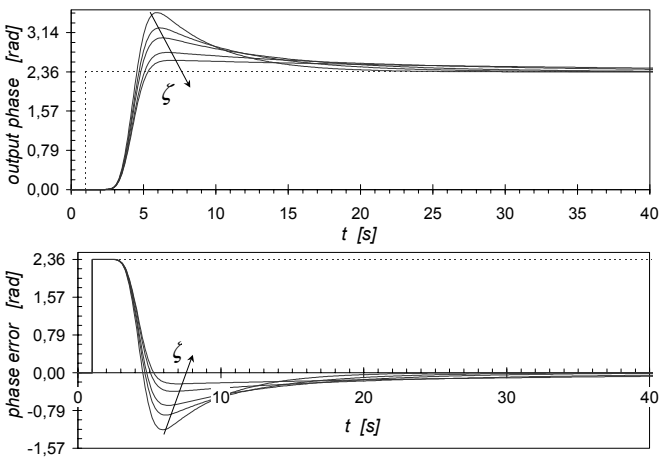

Fig. 10: Output phase and phase error of chains of N=20 SECs (B=1 Hz) with variable damping ratio ζ=3, 3.5, 4, 5, 7 (input phase step $\theta_{in}=(3/4)\pi$).

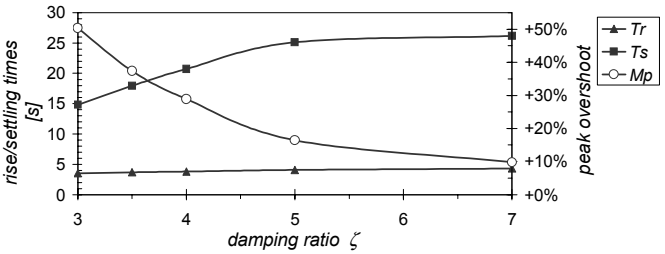

Fig. 11: Rise time T_r, settling time T_s and peak overshoot M_p of chains of N=20 SECs (B=1 Hz) with ζ=3, 3.5, 4, 5, 7 (input phase step $\theta_{in}=(3/4)\pi$).

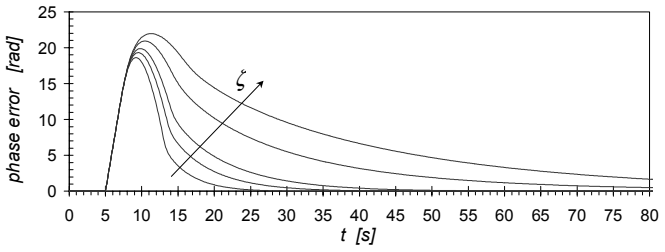

Fig. 12: Phase error of chains of N=20 SECs (B=1 Hz) with variable damping ratio ζ=3, 3.5, 4, 5, 7 (input frequency step $\Delta\omega_{in}$=6 rad/s).

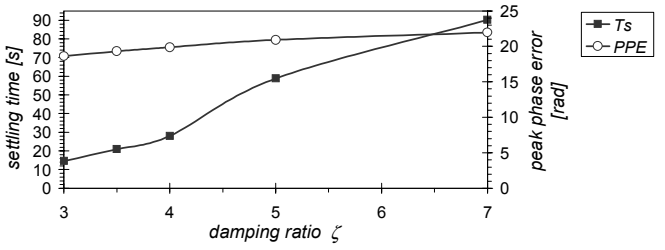

Fig. 13: Settling time T_s and peak phase error *PPE* of the output of chains of N=20 SECs (B=1 Hz) with ζ=3, 3.5, 4, 5, 7 (input freq. step $\Delta\omega_{in}$=6 rad/s).

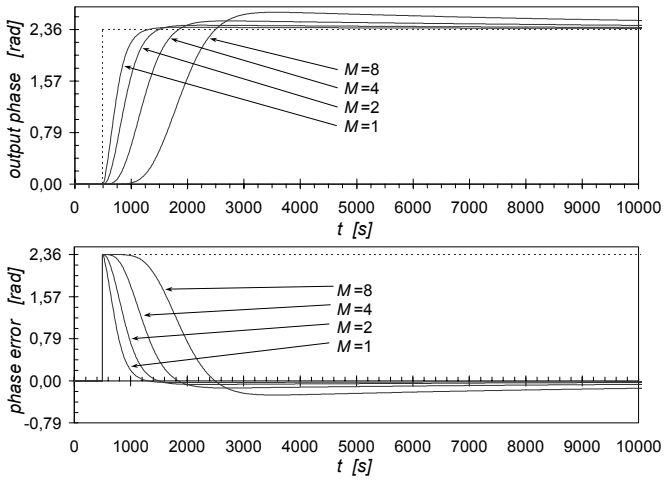

Fig. 14: Output phase and phase error of chains including M SASE clocks and N=20 SECs in each subchain (input phase step $\theta_{in}=(3/4)\pi$).

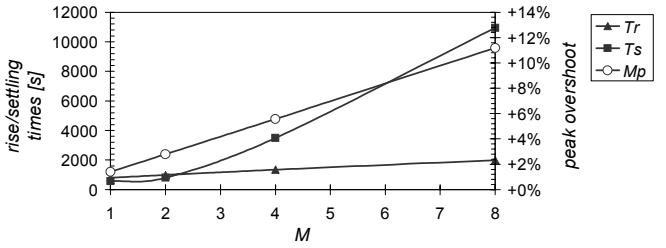

Fig. 15: Rise time T_r, settling time T_s and peak overshoot M_p of the output phase of chains including M SASE clocks and N=20 SECs in each subchain (input phase step $\theta_{in}=(3/4)\pi$).

A. Chains Including M *SASE Clocks and* N*=20 SECs in Each Subchain between Two SASE Clocks*

Chains including M=1, 2, 4, 8 SASE clocks (B=1 mHz, ζ=4, $\omega_n\cong 7.7\cdot 10^{-4}$ rad/s) with N=20 SECs (B=1 Hz, ζ=4, $\omega_n\cong 0.77$ rad/s) in each subchain between two SASE clocks have been studied. Their response to an input phase step starting at t=500 s and of amplitude $\theta_{in}=(3/4)\pi$ is shown in graphs of Fig. 14, which plot the output phase $\theta_{out}(t)$ and the phase error $\phi(t)$, respectively. Moreover, Fig. 15 plots the rise time T_r, the settling time T_s and the peak overshoot M_p.

By inspection, note first that transient duration and overshoot magnitude are determined by SASE, while SECs do not impact significantly on them. Note also that the settling time seems to increase more than linearly with the number of subchains, while the rise time and the peak overshoot exhibit linear dependence on it. Comparing this result to that of Fig. 7, the apparent different behavior is due to the different range of number of chained clock: $1\le M\le 8$ vs. $1\le N\le 40$.

Similarly, the response of the chains to an input frequency step starting at t=360 s and of amplitude $\Delta\omega_{in}$=6 mrad/s is shown in Fig. 16, which plots the phase error $\phi(t)$. Moreover, Fig. 17 plots the settling time T_s and the peak phase error *PPE* (both defined as for Fig. 9). Note the settling time increasing less than linearly with the number of SASE clocks, while the peak phase error still exhibits linear dependence on it.

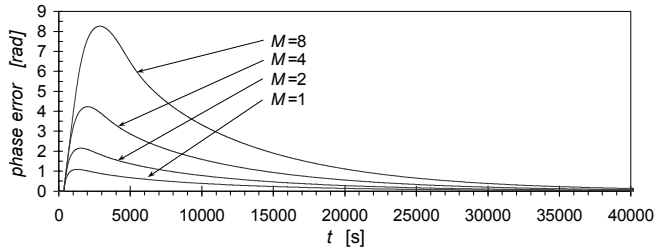

Fig. 16: Phase error of chains including M SASE clocks and N=20 SECs in each subchain (input frequency step $\Delta\omega_{in}$=6 mrad/s).

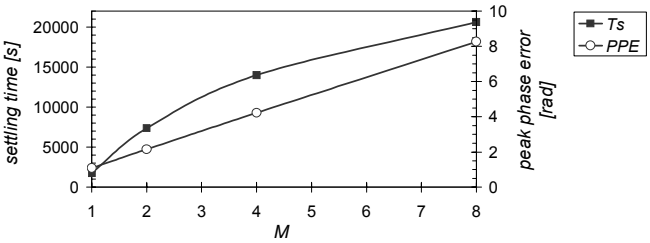

Fig. 17: Settling time T_s and peak phase error *PPE* of the output of chains including M SASE clocks and N=20 SECs in each subchain (input frequency step $\Delta\omega_{in}$=6 mrad/s).

B. Chains Including M *SASE Clocks and 80 SECs in Total*

Chains including M SASE clocks (B=1 mHz, ζ=4, $\omega_n\cong 7.7\cdot 10^{-4}$ rad/s) and 80 SECs (B=1 Hz, ζ=4, $\omega_n\cong 0.77$ rad/s) in total have been studied. These chains are made by cascading M+1 subchains, each made of N SECs and with one SASE clock between subchains as in Fig. 1, for (M=1, N=40), (M=3, N=20), (M=7, N=10) and (M=15, N=5).

The response of such chains to an input phase step starting at t=500 s and of amplitude $\theta_{in}=(3/4)\pi$ is shown in graphs of Fig. 18, which plot the output phase $\theta_{out}(t)$ and the phase error $\phi(t)$, respectively. Moreover, Fig. 19 plots the rise time T_r, the settling time T_s and the peak overshoot M_p.

By inspection, note again that the settling time increases with the number of SASE clocks in the chain, while the rise time and the peak overshoot exhibit linear dependence on it.

Similarly, the response of the chains to an input frequency step starting at t=360 s and of amplitude $\Delta\omega_{in}$=6 mrad/s is shown in Fig. 20, which plots the phase error $\phi(t)$. Moreover, Fig. 21 plots the settling time T_s and the peak phase error *PPE* (both defined as for Fig. 9).

Also in this case, note that the settling time increases less than linearly with M and the peak phase error linearly with it.

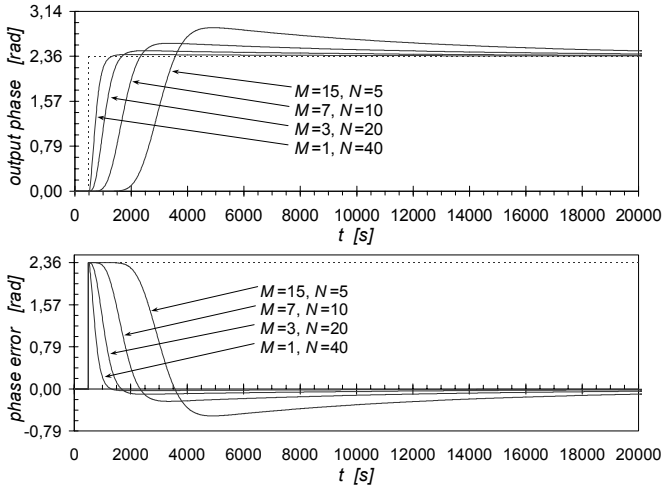

Fig. 18: Output phase and phase error of chains including M=1, 3, 7, 15 SASE clocks and 80 SECs in total (input phase step $\theta_{in}=(3/4)\pi$).

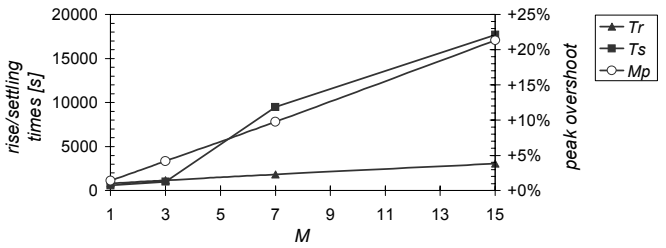

Fig. 19: Rise time T_r, settling time T_s and peak overshoot M_p of the output phase of chains including M SASE clocks and 80 SECs in total (input phase step $\theta_{in}=(3/4)\pi$).

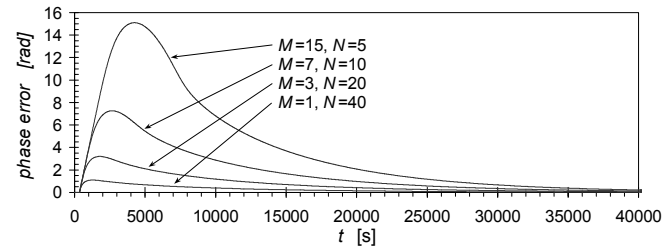

Fig. 20: Phase error of chains including M=1, 3, 7, 15 SASE clocks and 80 SECs in total (input frequency step $\Delta\omega_{in}$=6 mrad/s).

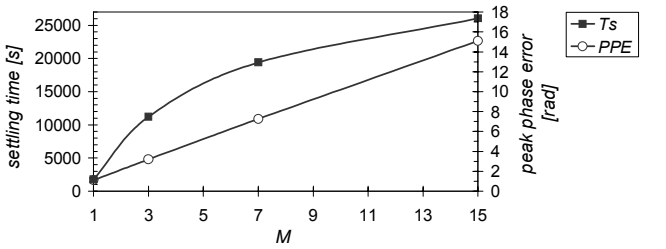

Fig. 21: Settling time T_s and peak phase error PPE of the output of chains including M SASE clocks and 80 SECs in total (input frequency step $\Delta\omega_{in}$=6 mrad/s).

VI. Conclusions

In this work, the non-linear transient behavior of SASE and SEC slave clock chains was simulated in the time domain, in order to evaluate their timing rearrangements after non-small phase and frequency hits on the reference signal.

Both homogeneous chains of SECs and non-homogeneous chains of SEC and SASE clocks have been studied in various configurations, thus providing synchronization engineers with a comprehensive survey, both in qualitative and quantitative terms, on the timing performance achievable when planning synchronization trails of various type and length. The following considerations stem from the results obtained.

- In chains of $1 \le N \le 40$ clocks, with input phase step, T_s increases less than linearly with N, while T_r and M_p exhibit linear dependence on it. Similar behavior is experienced with input frequency step.
- The clock damping ratio ζ affects both T_s and M_p in chains with input phase step, as it happens to a single clock. With input frequency step, ζ affects T_s but not substantially PPE.
- In chains including M SASE clocks and N SECs in each subchain between two SASE clocks, the response time scale is determined by SASE. With input phase step, T_s increases more than linearly with M (at least for small values of M, about few units), while T_r and M_p exhibit linear dependence on it. With input frequency step, T_s increases less than linearly with M, while PPE linearly with it.
- In chains including M SASE clocks and N SECs in total, with input phase step, again T_s increases with M, while T_r and M_p exhibit linear dependence on it. Similar behavior is experienced with input frequency step.

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