A Historical Perspective on Telecommunications Network Synchronization

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ABSTRACT Network synchronization, at first unknown and considered irrelevant to the operation and performance of telecommunications networks, has played an increasingly important role throughout the evolution of telecommunications, especially since transmission and switching became digital. This survey deals with telecommunications network synchronization from a historical point of view, aiming to show how network synchronization issues have evolved with telephone networks over the last 30 years, beginning with old FDM networks up to the latest technologies through PDH, SDH/SONET, and ATM. For each case, the different synchronization needs and the peculiar techniques of timing transfer and distribution are pointed out, thus providing a comprehensive overview of the evolution steps of telecommunications network synchronization.

Modern telecommunications networks are the result of a long evolution process, begun at the end of the 19th century.

Transmission and switching are the two basic functions of any telecommunications network, particularly telephone networks. *Transmission* deals with the transfer of information from one point in a network to another. *Switching*, on the other hand, deals with the dynamic assignment, on the basis of user connection requests, of the transmission channels available in the network. Transmission and switching are the complementary foundations on which all telecommunications services are based. Both transmission and switching were analog at first; then one after the other turned to digital technology.

The evolution of digital transmission and switching technology for public telephone networks began with isolated digital transmission links between analog switching machines or radio transmission systems. The fact that digital technology was used was transparent to the interfaces. Thus, there was no need to relate the internal clock rate in one system to the internal clock rate of another system.

Even as higher-level multiplexing systems were developed, there was no need (or viable means) to relate the clock rates of higher-rate multiplexed signals with those of lower-rate tributaries. Indeed, transmission equipment based on plesiochronous digital hierarchy (PDH) technology does not need to be synchronized, since a bit justification technique (pulse stuffing) allows multiplexing of asynchronous tributaries with substantial frequency offsets.

Problems began to arise with such asynchronous architecture when digital technology was adopted for switching machines too. Digital switching equipment requires synchronization in order to avoid slips in the elastic input stores. While slips do not significantly affect normal phone conversation, they may be troublesome indeed on some data services. The introduction of circuit-switched data networks and the integrated services digital network (ISDN), therefore, first yielded the need for more stringent synchronization requirements.

As a matter of fact, however, the ongoing spread of synchronous digital hierarchy (SDH) and synchronous optical network (SONET) technology in transmission networks has made synchronization a hot topic in standard bodies in the last few years, as the need for adequate network synchronization facilities has become more and more stringent in order to fully exploit SDH/SONET capabilities.

Beyond SDH/SONET needs, nowadays network synchronization facilities are indeed unanimously considered a profitable network resource, allowing slip-free digital switching, enhancing the performance of transport services based on asynchronous transfer mode (ATM), and serviceable for improving the quality of a variety of other services — ISDN, Global System for Mobile Communications (GSM), and so on.

For this reason, all the major network providers have set up or are now planning national synchronization networks in order to distribute a common timing reference to each node of their telecommunications networks. On the standardization side, the International Telecommunication Union — Telecommunication Standardization Sector (ITU-T) and European Telecommunications Standards Institute (ETSI) bodies are currently developing completely new synchronization standards, specifying more stringent — and complex — requirements for jitter and wander at synchronization interfaces, for clock accuracy and stability and for synchronization network architecture.

W. C. Lindsey *et al.* provided one of the main tutorials on network synchronization [1]. That article deals, from the theoretical point of view, with the distribution of time and frequency over a network of clocks located remotely, even with delay compensation, and presents mathematical models for characterizing synchronization networks, their stability, and their steady-state behavior. However, in the applications discussed in this article (i.e., mainly the synchronization of the equipment of digital telecommunications networks), delay compensation is not required because fixed phase offsets are not a concern.

On the other hand, P. Kartaschoff [2], writing a few years later, provides a quite general survey on various aspects of timing and synchronization in digital telecommunications networks, omitting all mathematical details. Basic concepts such as slips and synchronization network architectures and equipment are outlined.

A third tutorial article on digital network synchronization was written more recently by J. C. Bellamy in *IEEE Communications Magazine* [3]. That article is focused, on one hand, on the measure of jitter and wander and overviewing their main causes. On the other hand, the article deals with asynchronous and synchronous digital multiplexing and some timing aspects in such networks.

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This survey article deals, instead, with the synchronization of telecommunications networks from a historical point of view. After a short introduction to the main network synchronization strategies that have found the widest application, we show how the network synchronization issues evolved with telephone networks in the last 30 years, beginning with old frequency-division multiplexing (FDM) networks up to the latest technologies through PDH, SDH/SONET, and ATM. For each case, the different synchronization needs and peculiar techniques of timing transfer and distribution among the network nodes are pointed out, thus providing a comprehensive overview of the evolution steps of telecommunications network synchronization.

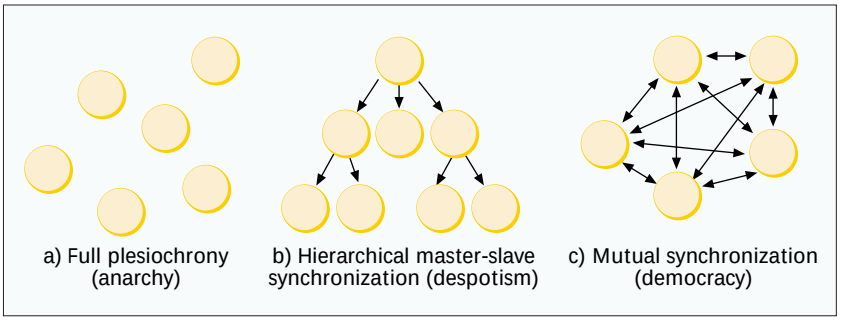

Figure 1. *Network synchronization strategies.*

Network Synchronization Strategies

Network synchronization deals with the distribution of time and frequency over a network of clocks, spread over an even wide geographical area [1]. The goal is to align the time and frequency scales of all the clocks by using the communications capacity of the links interconnecting them (e.g., copper cables, fiber optics, radio links).

Many intriguing examples of synchronization of a large number of oscillators can be found in nature. W. C. Lindsey *et al.* pointed out as one of the most spectacular ones the synchronous fireflies described by J. and E. Buck in their article cited in [1]. These fireflies flash their light organs at regular but individual and independent intervals if they are not close together; but if many of these insects are placed in a relatively close proximity, they exhibit a synchronization of their light organs until they flash in unison. Other biological examples are the synchronization of individual fibers in heart muscles to produce a familiar heartbeat, or the resting and active periods of mammals, which exhibit rhythms.

As advanced in the introduction, network synchronization plays a central role in modern digital telecommunications, determining the quality of most services offered by the network provider to its customers. To this purpose, many different network synchronization strategies have been conceived. Among them, the following three have found wide application throughout the last decades: full plesiochrony, hierarchical master-slave (HMS) synchronization, and mutual synchronization. The main features of these strategies will now briefly be reviewed, pointing out for each its socio-political analogy to help give an immediate understanding of its pros and cons.

Timing Relationships Between Digital Signals

An *isochronous* (from the Greek etyma ισος = *equal* and χρονος = *time*) digital signal is a digital signal in which the time intervals between significant instants have, at least on the average, the same duration or durations which are integer multiples of the shortest one. Standard digital signals are commonly isochronous (e.g., the HDB3-coded 2.048 Mb/s specified by ITU-T Rec. G.703).

Two *synchronous* (from the Greek etymon συγχρονος, built by συν = *with* and χρονος = *time*) digital signals are isochronous digital signals whose respective timing signals have the same frequency, at least on the average, and a phase relationship controlled precisely (i.e., with phase offset $\Delta\Phi$ kept constant). Conversely, two digital signals are *asynchronous* if they are not synchronous.

Two *mesochronous* (from the Greek etyma μεσος = *medium* and χρονος = *time*) digital signals are isochronous, asynchronous digital signals, whose respective timing signals have the same frequency, at least on the average, but no control on the phase relationship. It is worthwhile noticing that because the phase fluctuation function is the integral of the frequency fluctuation function, in this case the phase error $\Delta\phi$ is not theoretically limited over an infinite time interval even for small zero-mean frequency fluctuations.

Two *plesiochronous* (from the Greek etyma πλησιος = *close* and χρονος = *time*) digital signals are isochronous, asynchronous digital signals, whose respective timing signals have the same frequency values only nominally, but actually different within a given tolerance range.

Two *heterochronous* (from the Greek etyma ετερος = *different* and χρονος = *time*) digital signals are isochronous, asynchronous digital signals, whose respective timing signals have different nominal frequencies.

To give sound examples of the above abstract concepts, a locked Phase Locked Loop (PLL) outputs a timing signal which is synchronous with the input signal, owing to the feedback control on the phase error between them. A Frequency-Locked Loop (FLL), i.e., a feedback system operating like a PLL but instead controlling the frequency error between the input and the output signals, outputs a signal which is mesochronous with the input. Two oscillators, even if designed and built as equal by the same supplier, output two plesiochronous timing signals, owing to unavoidable manufacturing tolerances. Finally, two digital signals with different rates (e.g., 2.048 Mb/s and 8.448 Mb/s signals) are heterochronous.

Full Plesiochrony (Anarchy)

The plesiochronous strategy (see box 1) is actually a *no-synchronization* strategy (i.e., it does not involve any synchronization distribution). Each network node is equipped with an independent clock (Fig. 1a), hence the expression synchronization *anarchy*. Anarchy is the easiest form of government, but it relies on the good behavior of the single elements. Due to the lack of any timing distribution, the synchronization of operation of the different nodes is entrusted to the accuracy of the network clocks, which therefore must feature excellent performance.

As will be shown later, the full-plesiochrony strategy has been widely adopted in the past for FDM and PDH networks. In the late '60s, moreover, this strategy was generally considered also most promising for the future, due to the decreasing cost of atomic oscillators and the limited synchronization requirements of such transmission techniques. Nevertheless, since the cost of such oscillators became stable and the new digital techniques began to demand increasing timing performance, this strategy was eventually abandoned.

Hierarchical Master-Slave Synchronization (Despotism)

The principle of master-slave (MS) strategies is based on the distribution of the timing reference from a clock (*master*) to all the other clocks of the network (*slaves*), directly or indirectly (Fig. 1b).

EXPRESSING FREQUENCY ACCURACIES AND TOLERANCES

Frequency accuracies and tolerances are usually expressed in terms of the fractional frequency deviation $\Delta f/f_0$, where the frequency offset Δf is normalized to the nominal value f_0. Moreover, although ISO does not recommend it, it is quite common in telecommunications standards to specify such fractional frequency deviations in *parts per million* units (abbreviated as *ppm*), equal to 10^{-6}.

Despotism is generally considered unethical, but it is certainly effective in ensuring very tight control of the slaves: an MS network is synchronous with the master clock and stable by definition. Questions may arise, nevertheless, on what happens if the (unique) master fails. Therefore, HMS synchronization architectures are usually organized in two or more hierarchical levels and allow several protection mechanisms against link and clock failures.

The HMS strategy is currently the most widely adopted to synchronize modern digital telecommunications networks, due to the excellent timing performance and reliability that can be achieved at limited cost.

MUTUAL SYNCHRONIZATION (DEMOCRACY)

Mutual synchronization is based on direct *mutual control* among the clocks so that the output frequency of each is the result of the "suggestions" of the others (Fig. 1c). Such a pure democracy looks appealing: there are no masters and no slaves, but mutual cooperation. However, the behavior of the mutually controlled elements is hard to govern.

Modeling the behavior of such networks, or even ensuring the stability of the control algorithms, can be a very complex task [1, 4]. Networks so designed thus tend to be quite expensive, but textremely reliable. Therefore, until now the field of application of mutual synchronization has been mostly limited to special cases (e.g., military networks).

SYNCHRONIZATION IN ANALOG FDM NETWORKS

Until the introduction of digital techniques, any technological change had separate impacts on transmission and switching, two very distinct functions implemented in different pieces of equipment and experiencing different evolution processes. The introduction of FDM multiplexing techniques enormously enhanced the capacity of transmission links, without bringing significant changes in the operation principles, implementation techniques, or management and control systems of switching exchanges.

FDM is an *analog* standard technique allowing multiple channels to share a common physical medium. Since the '30s, its name has belonged to the history of telephone networks. FDM consists, as its name says, of shifting every tributary channel in the frequency domain to different locations in the spectrum $S_{MUX}(f)$ of the multiplex signal, so there are no channel interferences and it is thus still possible to separate single channels from the multiplex signal by bandpass filtering (Fig. 2).

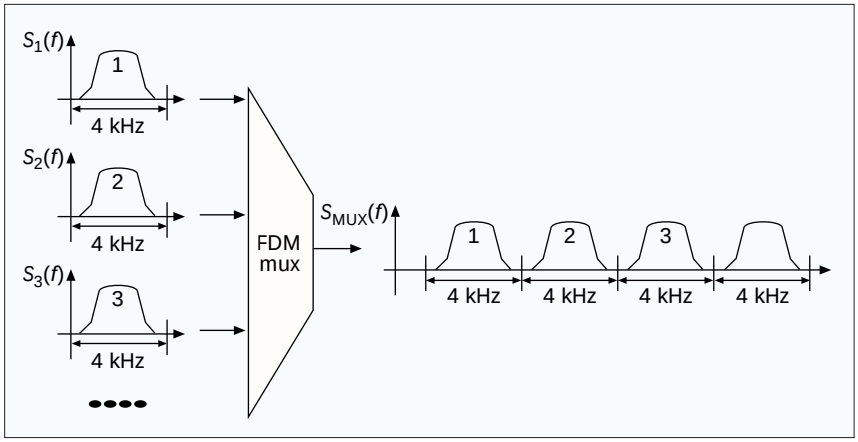

Figure 2. *Principle of frequency-division multiplexing of telephone signals.*

Frequency shifting of every channel is done through single-sideband (SSB) modulation of a sine wave (*carrier frequency*) and is done through subsequent multiplexing steps, according to a multiplexing hierarchy defined by CCITT (now ITU-T) Recommendation G.211. SSB demodulation must be *coherent*, that is, consists of multiplying the modulated signal by a sine wave with the same frequency and phase as the carrier and then low-pass filtering. Coherent demodulation is thus based on carrier reconstruction (*carrier synchronization*) [5] (i.e., the recovery of a signal coherent with the carrier in frequency and phase). More precisely, a frequency offset between the true carrier and that recovered yields phase and amplitude distortion of each component of the demodulated baseband signal; a phase offset, on the other hand, yields only phase distortion.

Carrier synchronization was accomplished in the first FDM systems through a simple point-to-point strategy, limited to each single transmission system (multiplexer/line system/demultiplexer). Later on, when FDM systems spread to constitute large networks, comprising links at different levels of the multiplexing hierarchy, the issue of an FDM network synchronization strategy had to be faced. While some network providers relied on a full-plesiochronous strategy, AT&T set up the first synchronization network in the '70s, according to an HMS architecture [6].

The strategy adopted was based on deploying *carrier supplies*, which is equipment generating all necessary carriers to be used by multiplexers and demultiplexers for all hierarchical levels, and on synchronizing them by distributing a *pilot frequency* (usually a multiple of 4 kHz) derived from a network master clock. Carrier supplies used phase-locked loops (PLLs) to synthesize reference frequencies synchronous with the pilot received.

The main task of those PLLs was, on one hand, to ensure adequate short-term stability by filtering phase fluctuations accumulated by pilots along the transmission links and, on the other, to provide in any case an output reference frequency, even under loss of the input pilot, by *free-running* operation of the local oscillator. Free-run frequency accuracy required to limit distortion in the demodulated signals was on the order of 10^{-7} (ITU-T Recommendation G.225) (see box 2). Such a frequency accuracy was enough to ensure adequate transmission quality of the telephone channels even under pilot frequency losses lasting the average time to restore.

SYNCHRONIZATION AND PDH DIGITAL TRANSMISSION

As stated before, when digital transmission in the very beginning was limited to isolated links between analog switching machines or radio transmission systems, there was no need to relate the internal clock rate in

one system with that of another. The need to best exploit the physical media then led to the development of digital time-division multiplexing (TDM) techniques, enabling multiplexing together thousands of telephone channels. Two options for digital multiplexing (i.e., multiplexing of digital tributary signals) are available: synchronous and asynchronous. Both may be bit- or byte-interleaved.

Synchronous Digital Multiplexing and Asynchronous Digital Multiplexing

In *synchronous digital multiplexers*, the tributary signals are assumed to be synchronous, with frequency in fixed ratio to the multiplex signal frequency. Therefore, the tributary bits can be mapped in fixed locations (carrying a fixed transmission capacity) in the multiplex frames. The unavoidable random fluctuations of the instantaneous frequencies around the mean value are absorbed by input buffers, designed large enough to compensate for the expected peak-to-peak phase deviations (see the "Synchronization and Digital Switching" section for further details on this mechanism, called *slip buffering*).

This optimal situation of synchronism among all the tributaries, assumed in the operation of synchronous digital multiplexers, has not been easily achievable for a long time. In *asynchronous digital multiplexers*, therefore, the tributary signals are assumed to plesiochronous instead, with frequencies not in fixed ratio to the multiplex signal frequency. This situation of plesiochrony is due to the fact that each piece of multiplexing equipment is assumed to work under the control of a local independent clock. Here, the adaptation of tributary signals into the multiplex signal is performed by means of a *bit justification* (also called *pulse stuffing*) technique, which allows multiplexing of asynchronous tributaries (bit-interleaved multiplexing is mostly used).

The Bit Justification Technique (Pulse Stuffing)

In synchronous digital multiplexers, the bits of each tributary are written in an input buffer (one buffer per input tributary), with write frequency equal to the incoming tributary instantaneous bit rate. The tributary bits are then read, according to the local equipment clock, and multiplexed by bit-interleaving. To cope with the issue of plesiochrony among different tributaries and the multiplex signal, which may make the buffers empty or full, certain bit positions within the output multiplex frame (*justification* or *stuffing opportunity bits*) can carry either tributary or dummy bits. In most standard frame formats, one justification opportunity position is reserved for each tributary in each multiplex frame.

The justification decision (i.e., if the stuffing opportunity bit should carry information or be a dummy) is made frame by frame on the basis of a buffer threshold mechanism. Therefore, the actual number of tributary bits in the output multiplex frame varies "on demand" and the transmission capacity (*each* transmission capacity allocated to each tributary multiplexed in the output signal, independently) gets adapted to the actual bit rate of the incoming tributary.

The term "justification" originated in the printing industry, where it describes the process of adjusting the spaces between printed words so that all the lines of print are the same length. Another practical example of justification is embodied by the concept of a leap year. A nominal-length calendar year is 365 days, but to make the calendar year nearly the same as the solar year an extra day is added to the year at the end of February once every four years; that is, every 4(365) days, a day is justified.

The presence or absence of stuffing bits in each multiplex frame must be properly signaled to the far-end demultiplexer in order to allow it to neglect the dummy bits in the reconstruction of tributary signals. To this purpose, special additional bits are inserted into the multiplex frame, called *stuffing* or *justification control bits*.

Plesiochronous Digital Hierarchy

In order to overcome the complexity of the issues related to synchronizing all the network nodes, the option of asynchronous digital multiplexing was chosen by the CCITT to establish the PDH standard, a series of standard bit rates (hierarchical levels) defined for transmission in digital telephone networks. Since the '70s, PDH has been the foundation of digital transmission systems in telephone networks worldwide.

Two plesiochronous hierarchies, with different bit rates but following the same principle, have been defined by the ITU-T through the years (ITU-T Recommendation G.702): the European and North American (with a Japanese variant) hierarchies. Both are based on bit-interleaved asynchronous digital multiplexing. The multiplex signals of the *i*th level ($i > 1$) are made by multiplexing a given number of signals of the $(i - 1)$th level. Tables 1 and 2 summarize the European and North American/Japanese PDH bit rates (the abbreviations E*i* and T*i*, to denote signals of the two hierarchies, respectively, are commonly used). It is worthwhile noticing that the T4 signal (274.176 Mb/s) of the North American hierarchy and the fifth-level signal (400.352 Mb/s) of the Japanese hierarchy have not been standardized by ITU-T.

The frequency offsets from the nominal value allowed in PDH tributaries are specified by ITU-T Recommendation G.703. As an example, for the PCM primary multiplex signal (having bit rate 2.048

Level	Nominal bit rate	No. of telephone channels carried
E1	2.048 Mb/s	30
E2	8.448 Mb/s	4 x 30 = 120
E3	34.368 Mb/s	4 x 120 = 480
E4	139.264 Mb/s	4 x 480 = 1920
E5	564.992 Mb/s	4 x 1920 = 7680

Table 1. *Summary of the European plesiochronous digital hierarchy.*

North American hierarchy			Japanese hierarchy		
Level	Nominal bit rate	No. of telephone channels carried	Level	Nominal bit rate	No. of telephone channels carried
T1	1.544 Mb/s	24	T1	1.544 Mb/s	24
T2	6.312 Mb/s	4 x 24 = 96	T2	6.312 Mb/s	4 x 24 = 96
T3	44.736 Mb/s	7 x 96 = 672	3rd	32.064 Mb/s	5 x 96 = 480
T4	274.176 Mb/s	6 x 672 = 4032	4th	97.728 Mb/s	3 x 480 = 1440
			5th	400.352 Mb/s	4 x 1440 = 5760

Table 2. *Summary of the North American and Japanese plesiochronous digital hierarchies.*

Mb/s and 1.544 Mb/s in the European and Japanese and North American hierarchies, respectively) a frequency tolerance of 50 ppm is specified. Bit justification thus allows accommodation of a variable number of tributary bits (about ±100 b/s and ±75 b/s, respectively) in the 8.448 Mb/s and 6.312 Mb/s multiplex frames.

Therefore, PDH transmission networks do not need to be synchronized, and the full-plesiochronous strategy can be adopted (synchronization anarchy). Every equipment clock is independent of the others, but their frequencies are just kept close to the nominal values within specified standard tolerance intervals.

Timing Transparency in PDH Systems

It is now important to point out that PDH systems are transparent to the timing content of transported digital signals. Referring, for instance, to the European hierarchy (as well as in the rest of the article for the sake of simplicity), a 2.048 Mb/s primary multiplex, multiplexed with three other asynchronous tributaries in a second-order multiplex, and then on into the upper PDH hierarchical level signals, when recovered at the end of the transmission chain has the same *average* frequency it had before the multiplexing/demultiplexing chain (with, of course, some jitter due to the transmission lines and some due to the pulse stuffing process, called *waiting time jitter* [7]), although the multiplexer clocks of the transmission chain are independent. The jitter and wander limits allowable at PDH interfaces are specified by ITU-T Recommendations G.823 and G.824.

This fact is remarkable indeed. The pulse stuffing technique allows the *transfer of the timing content* of a digital signal across a transmission chain where clocks are asynchronous instead, as shown in Fig. 3. There, thick grey links denote the signals which are synchronous with the master clock (i.e., transferring timing), while all others are asynchronous. A 2.048 Mb/s signal is generated by a digital switching exchange with the local clock driven by the network master clock. The multiplex signals (thick black links) are not synchronous with it, but due to pulse stuffing they embed the 2.048 Mb/s signal carrying timing. When the 2.048 Mb/s is recovered, it is still synchronous with the master clock. As will be shown in the next section, such a feature is exploited to transfer timing across PDH networks to synchronize clocks located in far locations.

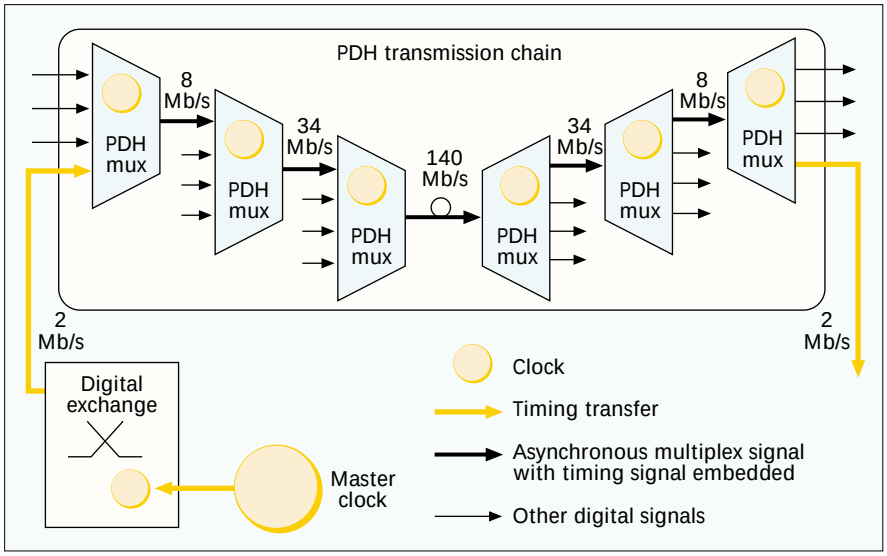

Figure 3. *Timing transfer through a PDH transmission chain.*

Synchronization and Digital Switching

The advent of digital TDM techniques yielded a progressive integration of transmission and switching, since the PCM primary multiplex frame structure allows exploiting of the TDM principle for digital switching of circuit connections as well.

Digital Switching Requires Time Alignment of the Input PCM Frames

The European 2.048 Mb/s PCM frame is made of 32 octets (time slots), 30 of which carry single 64 kb/s telephone channels, while the North American 1.544 Mb/s PCM frame is made of 24 slots. Digital switching is based on moving octets (speech samples) from one time slot to another, from one input signal to another output signal. Time slot exchanging is basically done by delaying, by a suitable time interval, the incoming octets before retransmitting them in the output frames at the right place (time).

It clearly appears that digital switching can take place *only* if incoming frames (asynchronous since they can be generated by different pieces of equipment with different clocks) are made synchronous, with frame starts aligned, so that correspondent time slots at different inputs are perfectly time-aligned. Therefore, one of the tasks of the input line units of a digital switching exchange is to synchronize bits and frames of incoming PCM signals before feeding them into the switching fabric, as outlined in Fig. 4. In this figure, for the sake of simplicity, only one frame per line is depicted (with alignment words shaded), and the time slot interchanging in the PCM frames is not pointed out.

Bit and Frame Synchronization by Means of an Elastic Store

Every incoming PCM signal is bit-synchronized according to the equipment local clock so that all incoming frames can then be time-aligned. Bit and frame synchronization are accomplished according to the principle depicted in Fig. 5, for each input line. The bits of the asynchronous PCM input signal are written into an elastic store (buffer) at *their* arrival rate f_w (none can obviously affect the far source clock), but are read at the equipment local clock frequency f_r.

This simple mechanism allows feeding the switching fabric with synchronous PCM frames and aligned frame starts. Note that a similar scheme, based on an elastic store, is used in synchronous and asynchronous digital multiplexers to absorb small random fluctuations of the tributary instantaneous frequencies and, through a threshold mechanism, to control justification when pulse stuffing is used (see the "Synchronization and PDH Digital Transmission" section). Note also, incidentally, that the terms *bit* and *frame synchronization* are often used in other contexts, with different meanings: the former may denote the clock recovery process from a binary signal to control the sampling and decision of the single binary symbols; the latter may denote the process of delineating the frames in the raw stream of received bits, based on a suitable strategy of hunting a known alignment word.

The elastic store absorbs any random

zero-mean frequency fluctuation between the write and read clocks, within given bounds due to buffer limits. Of course, any frequency offset $|f_w - f_r|$ between the write and read clocks will make the buffer empty or overflow, sooner or later.

SLIPS

The elastic store is implemented as a circular memory with cyclic access. If the buffer empties (i.e., the write and read memory addresses coincide because the read address overtakes the write address), some bytes are repeated in transmission. If the buffer overflows (i.e., the write and read memory addresses coincide because the read address is overtaken by the write address), some bytes are deleted and lost. Such events are called *slips* (hence the name *slip buffering* for this technique of bit synchronization). Repetitions or losses of an integer number of frames, thus maintaining frame alignment and limiting data loss, are called *controlled slips*.

The slip rate F_{slip} is a function of the number N of bits repeated or lost in one slip (obviously, the buffer size is not smaller than N) and of the frequency offset $|f_w - f_r|$. Expressing the frequency offset in hertz, the following simple relationship holds:

$$F_{slip} = 86{,}400 \frac{|f_W - f_r|}{N} [\text{slips / day}]$$

where the pure number 86,400 is the number of seconds in one day. In other words, a larger buffer allows reduction of the slip rate for any given clock accuracy.

However, even a buffer size up to a few frames with a frequency offset of 50 ppm, as specified by ITU-T G.703 for PCM primary multiplexes, would yield a slip rate not acceptable at all even for the simplest plain old telephone service (POTS). Since the introduction of the first telephone digital exchanges, therefore, the issue of controlling the slip rate was faced [8] by improving the accuracy of their clocks or through a suitable network synchronization plan. ITU-T Recommendation G.822 specifies the controlled slip rate to not exceed on an international digital connection.

SYNCHRONIZATION OF DIGITAL SWITCHING EXCHANGES THROUGH PDH LINKS

As said in the "Network Synchronization Strategies" section, in the beginning equipping digital exchanges with high-precision independent clocks (*full-plesiochronous strategy*) was generally preferred and considered the most promising solution, since few slips were tolerated for POTS and the cost of very accurate oscillators (quartz and atomic oscillators) was foreseen to progressively decrease. Later on, the introduction of more advanced data services (e.g., circuit-switched data networks) yielded the need for more stringent synchronization requirements and made network synchronization the only suitable strategy (usually according to an *HMS architecture*).

Digital exchange clocks are therefore usually synchronized by a reference master clock according to a suitable network synchronization plan. Timing is commonly transferred across PDH links, exploiting their timing-transparency property, as explained in the previous section (Fig. 3).

The scheme of synchronization of two digital switching exchanges through a PDH transmission chain is outlined in Fig. 6, where the same graphical notation of Fig. 3 holds. The clock of the first exchange is slaved to a master clock (traceable to the master clock of the whole digital exchange network), so all 2.048 Mb/s signals output by this exchange are synchronous. The equipment clock of the second exchange is synchronized by means of one of these 2.048 Mb/s signals (which may be carrying normal payload as well) assigned to transfer timing, which is transported across a PDH transmission chain from the first exchange to the second, multiplexed together with other signals.

A second scheme is based on the availability of a synchronization network based on the concept of *building* or *office clock*, which is a slave clock which serves an entire office by supplying timing to all the equipment deployed there, including digital switching exchanges, digital cross-connects (DXCs), and terminal equipment and multiplexers. Such clocks are referred to as *synchronization supply units* (SSUs) or

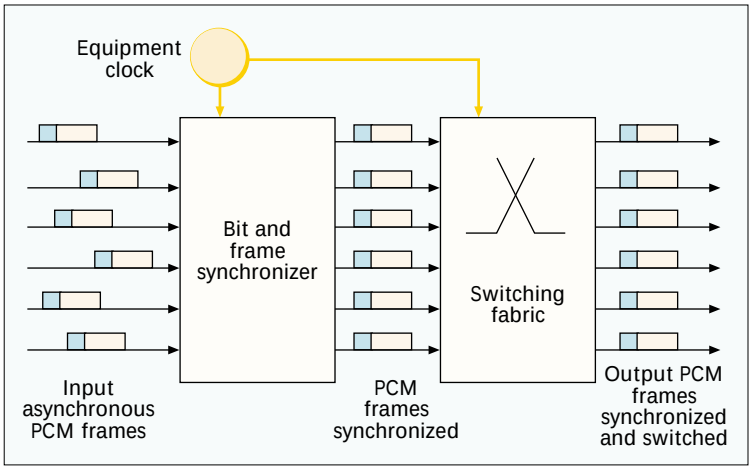

Figure 4. *Bit and frame synchronization of PCM signals at the input of a digital switching exchange.*

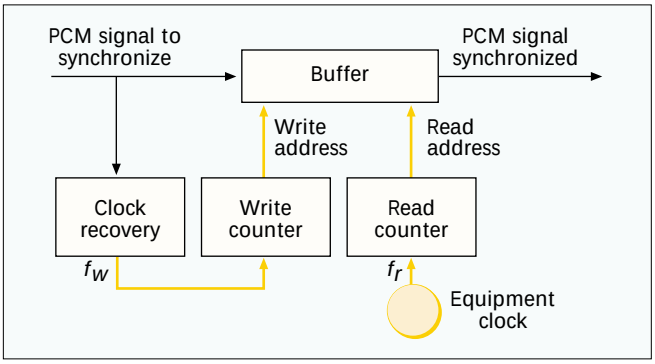

Figure 5. *Scheme of the principle of a bit synchronizer.*

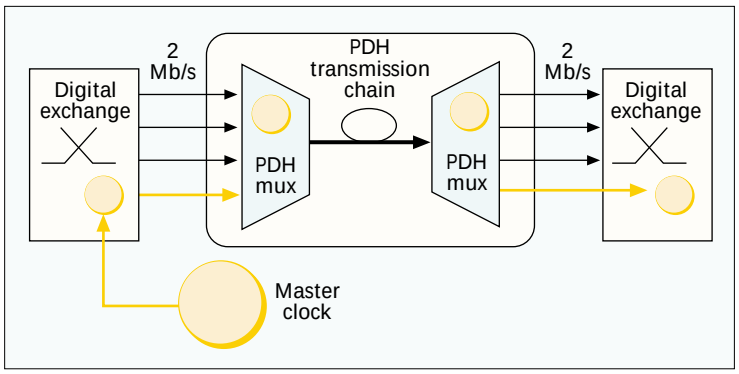

Figure 6. *Synchronization of two digital switching exchanges through a PDH transmission chain.*

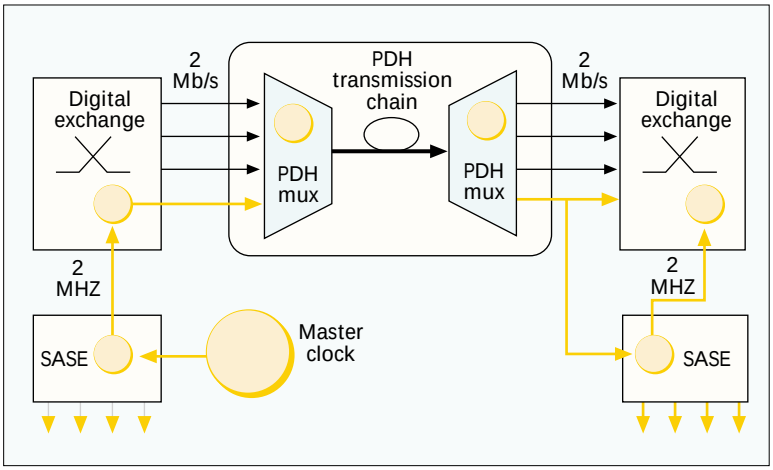

Figure 7. *Synchronization of two digital switching exchanges served by SASEs through a PDH transmission chain.*

standalone synchronization equipment (SASE) in the ITU-T and ETSI standards, and as building integrated timing supplies (BITS) in the American National Standards Institute (ANSI) standards.

This latter scheme is outlined in Fig. 7. The clock of the first digital switching exchange is synchronized by the local building clock (SASE), synchronized by the master clock and distributing timing to the equipment of the first office (usually by means of an ITU-T G.703 2.048 MHz signal). The clock of the second exchange is not directly slaved to a 2.048 Mb/s signal transported through the PDH transmission chain. Conversely, the 2.048 Mb/s signal carrying timing is used to synchronize the SASE which supplies timing to the equipment of the second office, including the switching exchange.

Since the late '70s and early '80s, the major world telecommunications providers have set up national network synchronization plans [9] to control slips in digital switching exchanges and DXCs, which are mostly based on the HMS strategy and on these two schemes of timing transfer from one digital exchange to another through PDH links.

Synchronization and SDH/SONET Digital Transmission

On 1988, the new standard transmission technique SDH was defined by the ITU-T, based on the ANSI standard SONET but with several extensions. Nowadays, SDH is progressively replacing PDH in backbone networks worldwide. The frames and signals of the SDH hierarchical levels are named *synchronous transport module* of level N (STM-N), for N = 1, 4, 16, 64. On the other hand, those of SONET are named *synchronous transport signal* of level N (STS-N), for N = 1, 3, 12, 48, 192. For reference, the standard hierarchical levels of SDH and SONET and their bit rates are summarized in Table 3. In the following, for the sake of brevity, we will refer simply to the ITU-T standard on SDH (G.707), understanding that all considerations apply to SONET as well.

Synchronous Multiplexing and Pointer Justification in SDH

The SDH frame structure is based on synchronous multiplexing of several building blocks (synchronous multiplexing elements) which are combined in various ways with complex rules. Such synchronous multiplexing elements are structured fixed-size sets of bytes, which are byte-interleaved or mapped one into the other to eventually form STM-N frames. Among them, virtual containers (VCs) are the basic building blocks and are conceptually the most innovative elements compared to the traditional PDH technique. A VC maps a payload, which can be any PDH signal as well as other lower-order synchronous multiplexing elements.

VCs are *individually* and *independently* accessible within SDH frames through *pointer* information directly associated with them by multiplexing. A pointer is located in a determined position within the containing multiplexing element (e.g., the STM-N frame) and identifies the position of the first byte of the pointed VC within the element (in this example, the frame itself).

When asynchronous SDH tributaries are fed into an SDH multiplexer, several VCs, timed by different clocks, are combined in one STM-N multiplex signal, timed by the local equipment clock. In order to compensate those frequency offsets, VCs are allowed to shift independently in the output STM-N frame. However, their position is always tracked by the respective pointers, which are incremented or decremented according to specified rules (ITU-T G.707). Such a mechanism is called *pointer justification* and is the SDH analogy to the bit justification mechanism of PDH. Nevertheless, VC shifting is allowed with much larger discrete steps, one or three bytes at a time according to the type of pointer. To stress the analogy with PDH, therefore, pointer justification is also called *byte justification*.

Output Jitter and Network Synchronization in SDH Systems

SDH systems are somehow transparent to the timing content of tributaries (e.g., 2.048 Mb/s) transported in the VCs. A digital signal, mapped in its VC and transported along an SDH transmission chain, has the same average frequency as before mapping when recovered at the end of the chain.

Nevertheless, contrary to what happens in PDH systems, here the jitter affecting the output tributary may be severe indeed. Besides the jitter due to the transmission line and waiting time jitter due to the mapping process into the VC, pointer justifications yield additional jitter due to the large discrete steps with which VC shifts happen [10, 11].

The actual amount of jitter at output tributary ports of SDH equipment depends on both the rate of pointer justifications taking place along the transmission chain and the particular design of the equipment itself. Although some modern equipment features an enhanced design [12] capable of substantially reducing the tributary output jitter even under heavy pointer action, the goal of guaranteeing jitter requirements (ITU-T G.823/4/5) at PDH/SDH boundaries in complex networks, where several PDH-to-SDH and SDH-to-PDH mapping/demapping processes take place and equipment of *different* vendors is deployed, can be achieved only by accurate synchronization of all the network elements aimed at avoiding any pointer action.

Therefore, contrary to PDH, SDH transmission takes advantage of network synchronization and may rely on it, depending on the implementation of equipment. Focusing on SDH needs, the international standard bodies have specified a standard synchronization network architecture, based on the SASE/BITS concept and the *HMS strategy* (ITU-T G.803, section 6). Such synchronization network architecture has been conceived and dimensioned for SDH needs, but should be considered valid in general for digital networks of any kind.

TIMING TRANSFER BETWEEN OFFICES THROUGH SDH LINKS

Timing transfer in SDH networks cannot follow the same schemes as in PDH. As stated above, in SDH networks the timing transparency of tributaries mapped in the multiplex STM-*N* frames is not as trustworthy; thus, it is definitely not advisable to carry timing on them due to their output jitter, which may be excessive, especially under pointer action.

However, the introduction of SDH technology in transmission networks allows more effective timing transfer between offices, because SDH equipment incorporates specific functions of timing generation, filtering, and extraction. The best and most straightforward way to transfer timing in SDH networks is to carry it directly on the multiplex STM-*N* signals. The quality of the timing recovered from STM-*N* signals is the best achievable today, affected only by transmission line jitter (e.g., jitter due to thermal noise and environmental conditions on the optical line), not by bit justification or any other mapping issue.

The scheme of synchronization of two digital switching exchanges through an SDH transmission chain is outlined by Fig. 8 (in which the same graphical notation as in Fig. 3 holds). Unlike the previous section, only the scheme based on the availability of a synchronization network with SASEs has been considered (Fig. 7), since it is deemed the target solution for synchronization networks as specified by ITU-T G.803.

The SASE in the first office synchronizes not only the digital switching exchange clock, but also the SDH equipment clock (SEC), so the output multiplex signal is now synchronous with the network master clock, contrary to the PDH case, where the multiplex signal was asynchronous but embedded the signal carrying timing. At the receiver side, the SEC is not directly locked to the incoming STM-*N* signal, as might seem natural. A special function of SDH equipment (defined by ITU-T G.783) instead allows the timing to be extracted from the incoming STM-*N* signal and directly output, not filtered, from the synchronization port (as a G.703 2.048 MHz signal) to synchronize the SASE of the second office. This SASE distributes its timing to the office equipment, including the digital switching exchange and SDH demultiplexer.

It is now worthwhile noting that this way of synchronizing the clocks of the second exchange may seem winding and unnecessarily complex, but it is definitely the best solution. Indeed, SASEs are clocks with much higher stability and filtering capabilities than simple SECs. Following this scheme, the clocks of the digital switching exchange and of the SDH (de)multiplexer in the second office are synchronized by a timing signal which is much more stable. Moreover, if the STM-*N* signal should fail, the SASE guarantees a long-term output frequency in free-running operation which is much more accurate than that of the SEC.

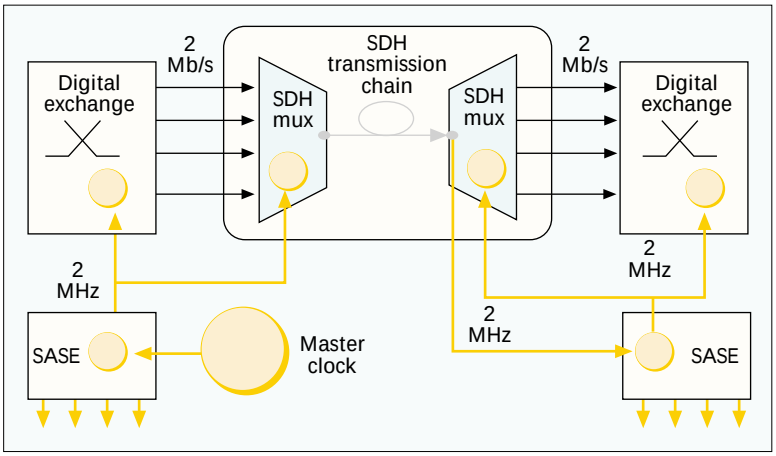

Figure 8. *Synchronization of two digital switching exchanges served by SASEs through a SDH transmission chain.*

SDH level	SONET level	Bit rate
(Sub-STM-1)[1]	STS-1	51.840 Mb/s
STM-1	STS-3	155.520 Mb/s
STM-4	STS-12	622.080 Mb/s
STM-16	STS-48	2488.320 Mb/s
STM-64	STS-192	9953.280 Mb/s

[1] The rate sub-STM-1 is defined only for the special case of radio transmission medium.

Table 3. *Hierarchical levels of SDH and SONET.*

SYNCHRONIZATION IN ATM TRANSPORT NETWORKS

There is a rather common misunderstanding about the role of synchronization in networks based on ATM, the cell-switched technique chosen by international standard bodies for the implementation of the broadband ISDN (B-ISDN). Since the first word in ATM is *asynchronous*, one is led to think that the natural operation of ATM equipment is in a nonsynchronous environment, in networks where clocks are independent and not synchronized.

Actually, the word "asynchronous" does not refer to the equipment clock operation, or to the *physical level* of information transfer, but to the information *transfer mode* instead, at an upper level of abstraction (the logic level of information transfer). In other words, it is pointed out that information sources are asynchronous, that is, they start sending information in independent instants, not in preassigned time slots as in synchronous transfer mode (STM, not to be confused with the same acronym denoting the SDH frame and meaning synchronous transport module), such as the PCM primary multiplex.

Contrary to this popular misunderstanding, synchronization plays an essential role in ATM networks, particularly in the integration of ATM equipment into existing telecommunications networks [13]. To summarize, ATM equipment requires synchronization mainly for two reasons:

- To support constant bit rate (CBR) services, based on ATM adaptation layer type 1 (AAL1) (ITU-T I.362 and I.363)
- To support synchronous physical interfaces, such as PCM primary multiplexes (2.048 Mb/s or 1.544 Mb/s) or SDH/SONET signals

As far as support of CBR services is concerned, the issue of packet jitter equalization in packet-switched networks to emulate circuit-like connections has been well known since before ATM [14]. Circuit-emulation CBR services indeed require that the timing of the carried service be maintained across the ATM network connection by properly equalizing the random delays of the cells received. To this purpose, the ITU-T accepted the synchronous residual time stamp (SRTS) timing recovery technique as the standard technique for AAL1 circuit emulation on ATM [15]. It must be pointed out that this technique relies on the availability, in the ATM equipment where AAL con-

nections are originated and terminated, of a synchronization signal traceable to a common network master clock.

On the other hand, supporting physical interfaces such as PCM primary multiplexes or SDH/SONET signals entails that the ATM equipment be able to be synchronized by means of an external network timing signal, in order to generate synchronous signals for ease of interworking with other equipment in the existing network.

For the above reasons, international standards (still evolving) require that ATM equipment accept external timing and be integrated into synchronization networks. Synchronization of modern ATM equipment is accomplished through dedicated ports (viz. 2.048 Mb/s, 1.544 Mb/s, or analog 2.048 MHz compliant with ITU-T G.703), while early ATM equipment did not feature such synchronization ports, since ATM synchronization requirements were not fully understood yet.

The most straightforward way to synchronize an ATM network element is to integrate it into a synchronization network based on the SSU/BITS concept. In such an environment, ATM equipment should take the timing reference from the SSU/BITS, which supplies by definition the most accurate timing signal available in the office. This allows, moreover, forgetting the burden of avoiding timing loops, which is a duty of the synchronization network manager.

SYNCHRONIZATION TODAY AND BEYOND

The underlying reason for the growing interest in network synchronization of the world's major network providers in the last few years is the awareness that network synchronization facilities are indeed a profitable network resource, which may be exploited to serve a wide range of equipment and services.

Controlling slips in digital switching networks through a suitable network synchronization plan became a strategic task as soon as POTS was no longer the only service provided, and more advanced data services such as circuit-switched leased lines or ISDN had been introduced. On the digital transmission side, the spreading of SDH/SONET technology has really made network synchronization a hot topic, since SDH transmission takes advantage of it. Moreover, the ongoing introduction of ATM in both the geographic and local areas is now causing further need for network synchronization. Other examples of modern digital services which may take advantage of the availability of network synchronization facilities are the GSM mobile phone and personal communications systems (PCS), which are based on a TDM technique for communication between mobile terminals and base stations.

The above and other examples show that a synchronization network is today considered a profitable general-purpose network resource, serving a variety of equipment and services. To make a long story short, the spreading of SDH enhanced the need for network synchronization in the '90s, but network synchronization is profitable for more than just SDH.

Deploying a modern synchronization network based on the SSU/BITS concept makes available, in every office of the telecommunications network, as many timing signals as required, with the greatest accuracy and traceable to a common network master clock, ready to serve equipment, services, or even customer premises. Today it is the usual policy of national network providers (e.g., public administrations) to provide customers' private networks, which utilize some digital transport service toward the rest of the world, with a timing signal traceable to the national reference in order to achieve error-free connection at switching interfaces between provider and customer networks. In a forthcoming scenario, indeed, even the timing itself might be sold as an advanced service to private network providers.

CONCLUSIONS

This survey article provides a comprehensive overview of the evolution steps of network synchronization from old FDM networks to the latest technologies through PDH, SDH/SONET, and ATM. For each case, the network synchronization strategies adopted and the different synchronization needs and techniques are pointed out. Moreover, this overview shows that a synchronization network is now considered a profitable general-purpose network resource, well beyond pure SDH needs.

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STEFANO BREGNI [M '93] (bregni@cefriel.it) received his Dott. Ing. degree in telecommunications engineering from the Politecnico di Milano, Italy, and his M.Sc. degree from the CEFRIEL Centre, Milano. In 1991 he joined SIRTI S.p.A., where he was mainly involved in SDH transmission systems testing and network synchronization issues, with special regard to clock stability measurement techniques. Since 1994 he has been with CEFRIEL, where currently he is head of the Transmission Systems Department. He served on ETSI and ITU-T committees on digital network synchronization and was guest editor of the *European Transactions on Telecommunications Focus on Synchronization of Digital Networks*. He is author or co-author of about 20 papers on several topics in this field, mostly published in IEEE conferences and journals.