Simulation of Clock Noise and AU-4 Pointer Action in SDH Equipment

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Abstract

One of the most important open issues in Standard Bodies dealing with synchronization of SDH networks is a better understanding of the impact of phase and frequency instabilities in Synchronous Equipment Clocks (SECs) on the statistics of pointer adjustments. In this paper, a flexible simulator of clock phase noise and of AU-4 pointer action is described. This simulator was designed with the aim of investigating how different spectra of SEC noise do impact on the statistics of AU-4 pointer adjustments. In particular, some results of simulations of different kinds of SEC noise obeying the power-law model are herein provided. Moreover, results of simulation of SEC noise fitting the ITU-T and ETSI standard mask specifying wander tolerance in terms of TDEV are herein reported.

1. Introduction

The introduction of the Synchronous Digital Hierarchy (SDH) [1] technology in the public transport digital networks, nowadays mainly based on the Plesiochronous Digital Hierarchy (PDH) [2], rises new important issues which have to be thoroughly investigated in order to fully exploit the SDH well known features. Among the other issues involved, the design of a suitable synchronization network plays a key role in determining the overall quality of any supported service. In particular, one of the most important open issues, both in academia and in standard bodies, is a better understanding of the impact of phase and frequency instabilities in SDH Equipment Clocks (SECs) on the statistics of pointer adjustments.

Pointers give the position of Virtual Containers (VCs), which map the user payload, in the synchronous frame structure. They allow payload fluctuations [3][4] in order to compensate phase and frequency offsets between the VCs originated at the head of the transmission chain and the SDH frames regenerated in every node. They are the underlying "magic" which allow synchronous multiplexing in a not perfectly synchronous network! Nevertheless, they are not flawless troubleshooters: every pointer adjustment is basically a sharp payload shift in the transport frame. In the case of AU-4 pointer, the Time Error (TE) between the local SEC and the one originating VCs is quantized at steps of about 160 ns (equivalent to three bytes of the VC-4 structure).

This can be a real issue in long chains of SDH equipment, where the timing is transferred along the chain and thus gathers phase impairments from every SEC. The cumulated effect of several pointer adjustments occurred along the chain may produce unacceptable output jitter values at the PDH/SDH boundaries [5], where the payload is demapped from its VC. This jitter may be reduced on one hand through a careful design of pointer processors, on the other with stricter requirements on the stability of SECs and - more generally - of network synchronization signals, in order to limit the occurrence rate of pointer adjustments.

Owing to the complexity of pointer processor algorithms and to the distinctive nature of the phase noise affecting timing signals, as it will be shown later, analytical models can be hardly conceived for studying the impact of SEC phase instabilities on the statistics of pointer adjustments. Simulation, instead, is almost always preferred because of its flexibility in modelling all kinds of pointer processors and thus its effectiveness in comparing their performance.

In this paper, a flexible simulator of clock phase noise and of AU-4 pointer action is described. This simulator was designed in order to investigate how different spectra of SEC noise do impact on the statistics of AU-4 pointer adjustments. Though the paper is focused on one particular model, the treatment is kept very general with the aim of providing also some tutorial guidelines for SEC noise and pointer processing simulation, useful to not well experienced readers too. In particular, the clock noise model is first introduced in Sec. 2, which deals with clock characterization. Then, the two basic modules of the simulator are described in Sec. 3: the generator of pseudo-random TE data and the pointer processor simulator module. Finally, some numerical results are shown in Sec. 4.

2. Clock Noise Characterization

In telecommunications, a *clock* is a device able to supply a timing signal, ideally periodic, usable for the control of telecommunication systems. A mathematical model describing an actual timing signal *s(t)* is given by [6][7]

$$s(t) = A \sin \Phi(t) \tag{1}$$

where *A* is a constant amplitude coefficient and $\Phi(t)$ is the *total instantaneous phase* expressed by

$$\Phi(t) = 2\pi(\nu_{\text{nom}} + \Delta\nu)t + \pi D \nu_{\text{nom}} t^2 + \varphi(t) + \Phi_0 \tag{2}$$

where $\Delta\nu$ represents the *frequency offset* of the actual clock from the *nominal frequency* ν_{nom}, *D* is the *linear fractional frequency drift* rate, mainly describing oscillator ageing effects, $\varphi(t)$ is the *random phase deviation,* modelling oscillator intrinsic phase noise sources, and Φ_0 is the initial phase offset.

The generated *Time* function T(*t*) of a clock is defined, in terms of its total instantaneous phase, as

$$\mathrm{T}(t) = \frac{\Phi(t)}{2\pi\nu_{\text{nom}}} \tag{3}$$

It is worthwhile noticing that for an ideal clock $\mathrm{T}_{\text{id}}(t)=t$ holds, as expected. Also the random phase deviation $\varphi(t)$ is often expressed in terms of time, as

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$$x(t) = \frac{\varphi(t)}{2\pi\nu_{\text{nom}}} \qquad (4)$$

Moreover, for a given clock, the *Time Error* function TE(t) between its time T(t) and a reference time $T_{\text{ref}}(t)$ is defined as

$$\text{TE}(t) = \text{T}(t)\text{-T}_{\text{ref}}(t) \qquad (5)$$

For a clock slaved to the reference timing signal, $x(t)$=TE(t) holds.

Main results deriving from theoretical analysis and experimental measurements show that most oscillators are typically affected by internal phase noise obeying the so-called *power law model* [7][8], in which the one-sided *Power Spectral Density* (PSD) $S_x(f)$ of $x(t)$ is described by a sum of terms, each varying as an integer power of the Fourier frequency

$$S_x(f) = \begin{cases} \sum_{\alpha=-4}^{0} m_\alpha f^\alpha & 0 \le f \le f_h \\ 0 & f > f_h \end{cases} \qquad (6)$$

where the m_αs are device-dependent parameters and f_h is an upper cut-off frequency. The most common noise types which dominate in precision oscillators are: *White Phase Modulation* (WPM) for α=0, *Flicker Phase Modulation* (FPM) for α=-1, *White Frequency Modulation* (WFM) for α=-2, *Flicker Frequency Modulation* (FFM) for α=-3, and *Random Walk Frequency Modulation* (RWFM) for α=-4.

The above frequency domain characterization, while it proves to be very meaningful and complete, on the other hand requires sophisticated measurement equipment and methodologies. Mainly for this reason, time domain techniques based on the use of digital counters have been developed. These techniques measure a sampled version of the function TE(t), starting from which various quantities characterizing frequency and time stability can be estimated. At present, five quantities are mainly considered in Standard Bodies for the specification of timing interfaces requirements [9][10]: the *Allan Deviation* (ADEV), the *Modified Allan Deviation* (MADEV), the *Time Deviation* (TDEV), the *root mean square of Time Interval Error* (TIErms), and the *Maximum Time Interval Error* (MTIE) [6][11][12]. All the frequency stability quantities are sensitive, with different ability, to the presence of the power-law noises in a timing signal [13].

3. The Simulator Engine

The simulation of AU-4 pointer action in SDH equipment involves two basic steps. The first step is to simulate phase instabilities in the SDH equipment clock, according to a suitable model such as the power-law (6) for the phase noise spectrum. Since the pointer processor "reads" the TE values at discrete intervals, i.e. basically when it has to generate the new pointer value, it is quite natural to adopt a discrete-time simulation technique. The output of this step is thus a pseudo-random sequence of TE samples, with length, sampling period and power spectrum properly chosen by the user.

The second step is then to input this sequence to the pointer processor simulator module, and to take note of pointer adjustments when they occur. The pointer processor can be modelled in different ways, according to the different implementations designed by SDH equipment suppliers [14] and to the level of approximation considered.

Both stages are implemented as independent software modules. Changes in the algorithm of generation of pseudo-random TE sequences do not impact on the design of the pointer processor module; likewise, the actual pointer processor model does not impact in any way on the design of the first stage.

3.1. Generation of Time Error Data

The task of the first stage of the simulator is to generate a pseudo-random sequence $\{x_n\}$ of N TE samples, spaced τ_0 seconds and with custom power spectrum $S_x(f)$.

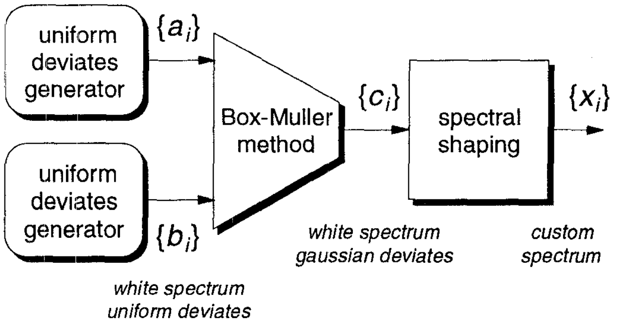
uniform deviates generator
$\{a_i\}$
uniform deviates generator
$\{b_i\}$
Box-Muller method
$\{c_i\}$
spectral shaping
$\{x_i\}$
white spectrum gaussian deviates
custom spectrum
white spectrum uniform deviates

Fig. 1: Generation of the pseudo-random sequence of TE samples $\{x_i\}$

The generation algorithm is outlined in Fig. 1. First, two independent sequences $\{a_i\}$ and $\{b_i\}$ of N *uniform deviates*, i.e. random numbers uniformly distributed and with negligible correlation between them (white spectrum), are generated. One sequence $\{c_i\}$ of N white *Gaussian deviates* is then computed through the following transformation (Box-Muller method [15])

$$\begin{cases} y_{i1} = \sqrt{-2\ln a_i}\cos 2\pi b_i \\ y_{i2} = \sqrt{-2\ln a_i}\sin 2\pi b_i \end{cases} \qquad (7)$$

by choosing any of the two sequences $\{y_{i1}\}$ and $\{y_{i2}\}$ as $\{c_i\}$.

Spectral shaping of the white-spectrum sequence $\{c_i\}$ is then accomplished through Fast Fourier Transform (FFT), by filtering with suitable transfer function H(f_n) so that

$$|\text{H}(f_n)|^2 = \frac{\breve{S}_x(f_n)}{K} \qquad (8)$$

where $\breve{S}_x(f_n)$ denotes the two-sided PSD and K is a normalization factor, to finally yield the sequence $\{x_i\}$. In this case, indeed, the burden of convolution algorithms such as overlap-and-add and zero-padding methods [15] is unnecessary, since the only constraint is to get a sequence just having the custom power spectrum $S_x(f)$. The resulting procedure can be thus really straightforward: $\{c_i\}$ data set is just crammed into computer memory, FFTed, multiplied sample-by-sample by $\{H_n\}$ and inversely transformed back to yield $\{x_i\}$.

3.2. AU-4 Pointer Processor Model

Pointer processors are specified by ITU-T [3] with a *functional* approach, i.e. it is specified at a very basic level what pointer processors should do, but the device implementation is not constrained to any particular design. Therefore, SDH equipment designers are free to conceive any trick to improve the resulting jitter performance. This yielded to different - but IUT-T compliant -

implementations of pointer processors [14]. Nevertheless, for the sake of simplicity, this paper deals with a basic model directly derived from ITU-T Rec. G.783 [3], leaving more detailed modelling or simulation of enhanced implementations for further study.

The AU-4 pointer processor model is outlined in Fig. 2. The bits of the incoming VC-4 are written into the elastic store (VC-4 buffer) with the clock signal generated by the upstream SEC, which is supposed ideal, and read out with the local noisy clock. In real equipment, write and read clock signals are derived by opportunely inhibiting (GAP block) the 155.520 MHz STM-N regular clock. Herein, a simplified model was assumed: GAP blocks, which inhibit the regular CK signals in correspondence of Section OverHead (SOH) bits, are rendered by simply averaging down the CK frequencies to about 150 MHz; for most considerations, anyway, this is not an oversimplification. If the TE between the write and read clock exceeds one of two buffer thresholds (THR block) spaced 12 bytes (equivalent to about 640 ns), then a positive or negative pointer adjustment takes place: both thresholds are moved 3 bytes (i.e. about 160 ns) upwards or downwards and the actual TE between clocks is updated by the same amount (I/D block).

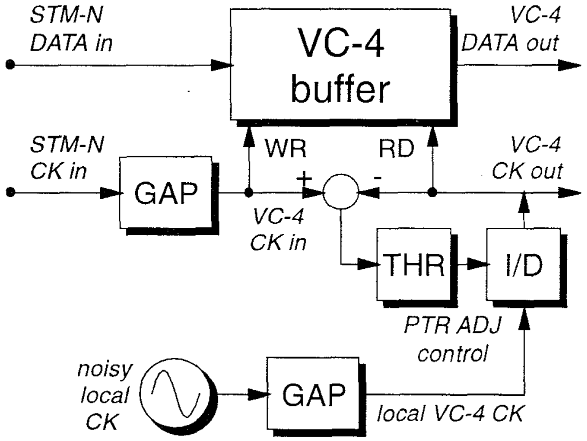

Fig. 2: AU-4 pointer processor model

4. Simulation Results

In order to investigate how different spectra of SEC noise do impact on the statistics of AU-4 pointer adjustments, several simulations were carried out (see also [16]). This paper first shows some results of simulations of different kinds of SEC noise obeying the power law (6), accomplished with the aim of understanding if SEC noises of type WPM, FPM, WFM, FFM and RWFM yield to different dynamics of AU-4 pointer adjustments. Moreover, results of simulation of SEC noise fitting the TDEV mask specifying wander tolerance, proposed in ETSI and ITU-T standards dealing with SECs [10][17], are herein reported. All the simulations were accomplished generating null-mean sequences of N=2^{24}=16777216 TE samples spaced τ_0=500 μs (thus covering a period T=2 h 20' of SDH equipment operation) corresponding to 4 STM-N frames.

4.1. Power-Law Noise

Ten different simulations for each of the five types of power-law spectrum were accomplished, with the aim of improving the confidence of results. Moreover, in order to appreciate the impact of different spectra, some measure of the TE fluctuations being equal, all the TE sequences were normalized, so to have the same root mean square (rms) value

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} \qquad (8)$$

set to σ=100 ns. As an example, Figs. from 3 to 7 show five of these TE sequences, respectively affected by WPM, FPM, WFM, FFM and RWFM noise. Of course, for ease of graphical representation, the curves shown depict only 4096 points, chosen by evenly sampling the full sequences.

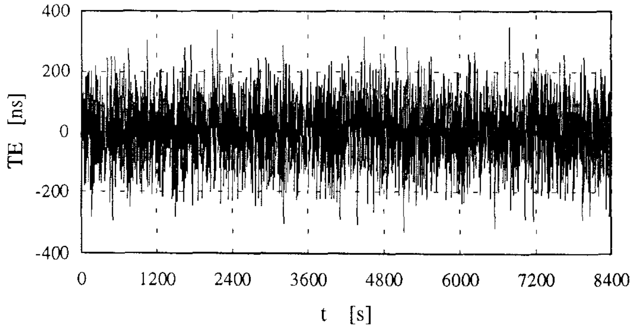

Fig. 3: WPM noise sequence

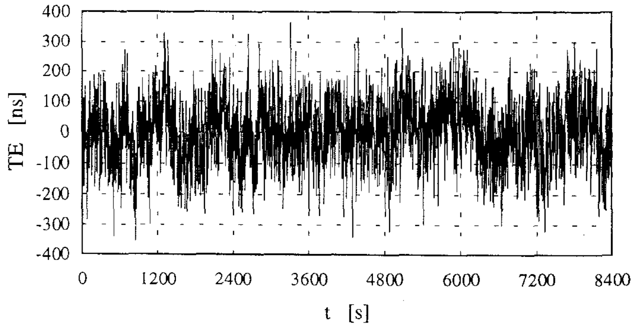

Fig. 4: FPM noise sequence

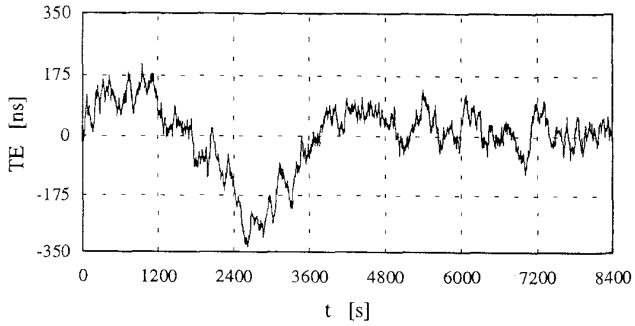

Fig. 5: WFM noise sequence

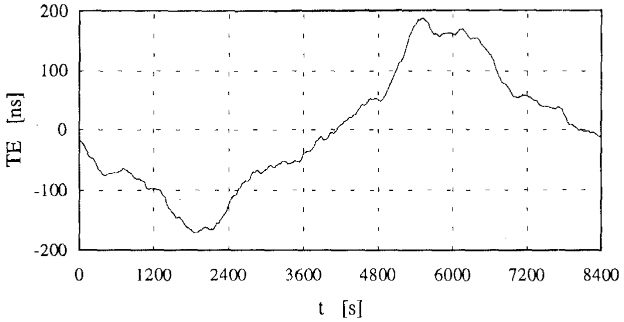

Fig. 6: FFM noise sequence

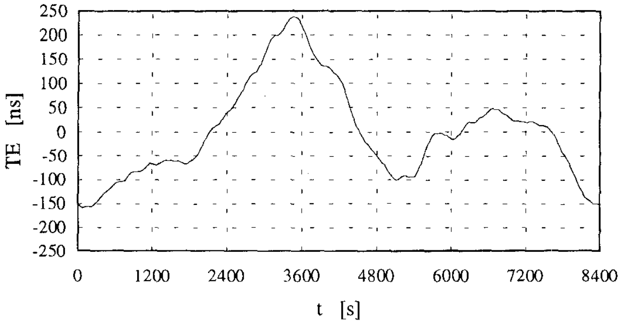

Fig. 7: RWFM noise sequence

It is quite interesting to point out that, as shown in Figs. from 3 to 7, the realizations of the process TE(t) are as smoother as the parameter α in (6) is decreased. In fact, any f^{α} noise can be viewed as a $f^{\alpha+1}$ noise filtered through a half-order integrator [18] with transfer function $H_{1/2}(f)=1/\sqrt{j2\pi f}$, and thus Figs. from 3 to 7 show indeed what happens by repeatedly integrating a white noise. Moreover, it clearly appears that, stepping from WPM to RWFM noise, waveforms get closer to a sine wave of period equal to the sequence length T. The reason is that, whatever T may be, the first harmonic at frequency $1/T$ is always $2^{-\alpha}$ times greater than the second at frequency $2/T$ (i.e., 8 times for FFM and 16 for RWFM), and so on for the next ones. Finally, the theory ensures that Gaussian processes through linear filters remain Gaussian, but the sine-like FFM and RWFM noises of Figs. 6 and 7 are - to the naked eye - quite far from exhibiting a Gaussian distribution. The bug lies in assessing the distribution of just *one* realization of the RWFM random process: one realization is not Gaussian, whereas the random process (which can be seen as a set of infinite realizations evolving parallely) is.

Pointer action resulting from these fifty simulations is summarized in the bar diagram of Fig. 8. Results are arranged in five rows (one for each noise type) of ten simulations, while the number of occurred pointer adjustments, counted by inputting the TE sequence to the pointer processor module, is on the vertical axis. It clearly appears the huge disparity of the number of pointer adjustments between the five rows of simulations, which reflects the different speed of processes: while the rms value is kept constant, WPM noise fluctuates faster than others.

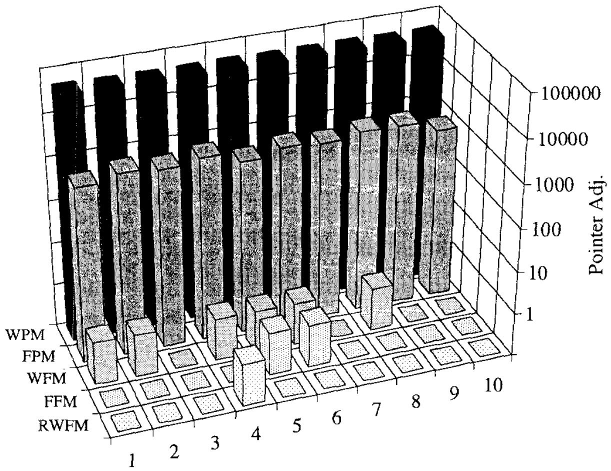

Fig. 8: Number of pointer adjustments vs. noise type in fifty simulations

4.2. Noise Fitting the TDEV Standard Mask for Wander Tolerance

ITU-T and ETSI standards currently include a TDEV mask for specifying the wander tolerance of SECs [10][17]. This mask is intended to represent the maximum cumulative network wander at the SEC input, i.e. for the synchronization inputs the required wander tolerance should be equal to the network limit. A phase noise fitting this TDEV limit was simulated by generating TE sequences with power spectrum

$$S_x(f)=\frac{G\left(1+f^2/Z^2\right)}{f\left(1+f^2/P^2\right)} \qquad (10)$$

where $G=8\cdot10^3\ \mathrm{ns}^2$, $P=4.5\cdot10^{-3}$ Hz and $Z=4\cdot10^{-2}$ Hz. Fig. 9 shows the excellent matching between the TDEV standard mask referenced above and the TDEV(τ) curve (thicker line) as computed from a TE sequence generated with PSD (10). This sequence is shown in Fig. 10; also here, for ease of graphical representation, only 4096 points are depicted, chosen by evenly sampling the full sequence.

The sequence shown in Fig. 10 produces 48 AU-4 pointer adjustments (contrary to before, in this simulation the local clock is supposed ideal while the input timing signal is carrying noise); other simulations with the same PSD (10) yielded to results around this value. Hence, it should be pointed out that such a network wander at SEC input allows substantial pointer action, and that stricter requirements are suggested if pointer action should be better controlled.

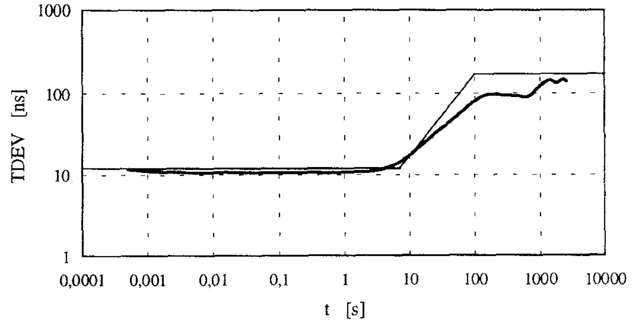

Fig. 9: TDEV standard mask vs. TDEV(τ) curve (thicker line) as computed from the generated noise sequence

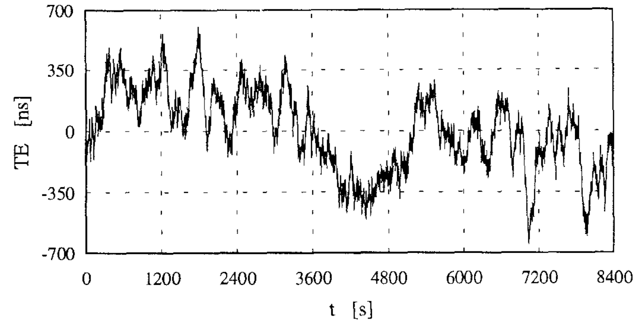

Fig. 10: TE sequence fitting the TDEV standard mask

5. Conclusions

A flexible simulator of clock phase noise and of AU-4 pointer action was herein described. This simulator has proved very useful for gaining more insight on how different spectra of SEC noise do impact on the statistics of AU-4 pointer adjustments. In particular, some results of simulations of different kinds of SEC noise obeying the power-law model were provided, together with results of simulations of noise fitting the TDEV standard mask for wander tolerance. These simulation results show that such a network wander at SEC input allows substantial pointer action, and that stricter requirements are suggested if pointer action should be better controlled.

References

[1] ITU-T Revised Rec. G.707 *"Synchronous Digital Hierarchy Bit Rates"*, G.708 *"Network Node Interface for the Synchronous Digital Hierarchy"*, G.709 *"Synchronous Multiplexing Structure"*, Geneva, 1993

[2] ITU-T Rec. G.702 *"Plesiochronous Digital Hierarchy"*, Blue Book, 1988

[3] ITU-T Rec. G.783 *"Characteristics of Synchronous Digital Hierarchy Equipment Functional Blocks"*, Geneva, March 1993

[4] M. Sexton, A. Reid, *"Transmission Networking: SONET and the Synchronous Digital Hierarchy"*, Norwood, MA: Artech House, 1992

[5] S. Bregni, M. D'Agrosa, L. Valtriani, *"Jitter Testing Technique and Results at VC-4 Desynchronizer Output of SDH Equipment"*, IEEE Transactions on Instrumentation and Measurements, Vol. IM-44, No. 3, June 1995

[6] J. A. Barnes, A. R. Chi, L. S. Cutler, D. J. Healey, D. B. Leeson, T. E. McGunigal, J. A. Mullen Jr., W. L. Smith, R. L. Sydnor, R. F. C. Vessot, G. M. R. Winkler, *"Characterization of Frequency Stability"*, IEEE Transactions on Instrumentation and Measurements, Vol. IM-20, No. 2, May 1971

[7] J. Rutman, F. L. Walls, *"Characterization of Frequency Stability in Precision Frequency Sources"*, Proceedings of the IEEE, Vol. 79, No.7, pp. 952-960, July 1991

[8] V. F. Kroupa, *"Noise Properties of PLL Systems"*, IEEE Transactions on Communications, Vol. Com-30, No. 10, October 1982, pp. 2244-2252

[9] ITU-T SG13/WP4/Q21 Rapporteur, *"Report of Expert Meeting on Synchronization"*, Rome, December 1993

[10] ETSI Draft ETS DE/TM-3017 *"Generic Requirements for Synchronisation Networks"*, Rome, October 1994

[11] P. Lesage, T. Ayi, *"Characterization of Frequency Stability: Analysis of the Modified Allan Variance and Properties of its Estimate"*, IEEE Transactions on Instrumentation and Measurements, Vol. IM-33, No. 4, December 1984

[12] S. Bregni, *"Facing up to Practical Measurement of MRTIE: a New Effective Methodology"*, Proceedings of ICC '95, Seattle, USA, June 1995

[13] S. Bregni, M. Carbonelli, D. De Seta, D. Perucchini, G. Zampilloni, *"Clock Stability Measure Dependence on Time Error Sampling Period"*, Proceedings of GLOBECOM '94, S. Francisco, USA, December 1994

[14] M. J. Klein, R. S. Urbansky, *"SONET/SDH Pointer Processor Implementations"*, Proceedings of GLOBECOM '94, S. Francisco, USA, December 1994

[15] W. H. Press, B. P. Flannery, S. A. Teukolsky, W. T. Vetterling, *"Numerical Recipes in C: the Art of Scientific Computing"*, 2nd edition, Cambridge University Press

[16] S. Bregni, L. Valtriani, F. Veghini, *"Impact of Clock Stability Recommended Masks on SDH AU-4 Pointer Adjustments"*, COMCON5, Chania, Greece, June 1995

[17] ITU-T New Draft Rec. G.81s *"Timing Characteristics of Slave Clocks Suitable for Operation of SDH Equipments"*, Geneve, November 1994

[18] J. A. Barnes, D. W. Allan, *"A Statistical Model of Flicker Noise"*, Proceedings of the IEEE, Vol. 54, No. 2, pp. 176-178, February 1966