Synchronization Processes and Jitter Generation along a SDH Transmission Chain: a Review and Measurement Results

STEFANO BREGNI
Dept. of Electronics and Computer Science
Politecnico di Milano
P.zza L. Da Vinci 32, 20133 Milano
ITALY
bregni@elet.polimi.it http://www.elet.polimi.it/~bregni

Abstract: - New timing issues have been raised by Synchronous Digital Hierarchy (SDH), which implies new phenomena generating jitter and wander compared to those well known in legacy networks based on the Plesiochronous Digital Hierarchy (PDH). First, this paper reviews the bit and byte synchronization processes that take place in a SDH transmission chain: the mapping of PDH tributaries into SDH frames, the re-synchronization of Virtual Containers (VCs) in intermediate nodes, the demapping of PDH tributaries from SDH frames. Then, this paper reviews the main causes of jitter and wander in a SDH transmission chain, by outlining the different phenomena that may affect the phase of the tributaries transported. First, the diurnal and annual wander due to variations of environmental conditions (temperature) is considered. Then, the jitter and wander caused by inclusion of additional bits in the mapping of tributaries into STM frames, by bit justification and by pointer justification is addressed. Finally, real measurement results of phase hits caused by AU4 pointer adjustments on a commercial SDH system are also provided, to provide experimental support to the general treatise.

Key-Words: - digital communication, jitter, pointer, SDH, SONET, synchronization, wander.

1 Introduction

The Synchronous Digital Hierarchy (SDH) [1][2] technique poses peculiar timing issues, which deserve a close look. Its introduction gave a new perspective on network synchronization [3]—[6] and yielded the need of a deeper insight, changing for example many of the original assumptions used in deriving parameters and limits to verify network synchronization quality. Moreover, new timing issues have been raised by SDH, which implies new phenomena generating jitter and wander compared to those well known in legacy networks based on the Plesiochronous Digital Hierarchy (PDH) [7][8].

First, this paper reviews the bit and byte synchronization processes that take place in a SDH transmission chain: the mapping of PDH tributaries into SDH frames, the re-synchronization of Virtual Containers (VCs) in intermediate nodes, the demapping of PDH tributaries from SDH frames. Each of these processes features peculiar issues.

Actually, in spite of the numerous advantages offered by SDH compared to PDH, SDH made the issue of controlling the jitter and wander on the transported tributaries more delicate than in traditional PDH networks. Therefore, this paper then reviews the main causes of jitter and wander in a SDH transmission chain, by outlining the different phenomena that may affect the phase of the tributaries transported. Wander due to variations of environmental conditions (temperature) and imperfect clock recovery in line regenerators may affect the phase of the whole SDH signals transmitted along the chain. SDH multiplexers, on the other hand, feature processes that generate jitter and wander solely on the tributary signals mapped. Such processes include: inclusion of additional bits in the mapping of tributaries into STM frames, bit justification to map the asynchronous tributaries into synchronous VCs, pointer justification which allows VCs to shift within other VCs or STM frames.

2 Synchronization Processes along a SDH Transmission Chain

In this section, the different bit and byte synchronization processes that take place in a SDH transmission chain are summarized. Fig. 1 shows a typical PDH-SDH-PDH path: a PDH tributary is mapped in the SDH frames and transported along a transmission chain made of *M* SDH Network Elements (NEs) until it is extracted by the terminating demultiplexer. Three synchronization processes take place in the SDH network elements of this scheme:

- the mapping of the PDH tributary into SDH frames in the first multiplexer (SDH NE #1),
- the re-synchronization of the VCs in the intermediate NEs along the SDH transmission chain,
- the demapping of the PDH tributary from SDH frames in the terminating demultiplexer (SDH NE #*M*).

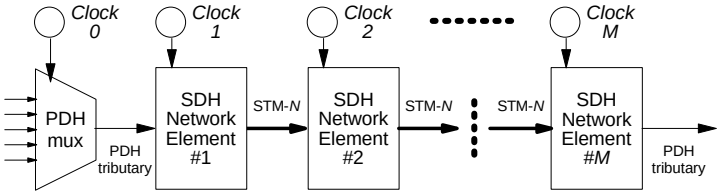

Fig. 1: Transport of a PDH tributary along a transmission chain made of *M* SDH network elements.

2.1 Mapping of PDH Tributary into SDH Frames

The PDH tributary signals at the input of SDH multiplexers are typically asynchronous. The adaptation of the bit rate of the PDH tributary (clock 0 in Fig. 1) to the bit rate of the mapping SDH VC (clock 1 in Fig. 1) is performed, as in PDH multiplexers, by means of *bit justification*.

The VCs based on asynchronous mapping are made of tributary bits (true payload), miscellaneous overhead, fixed stuffing, justification opportunity bits and justification control bits. The functional block carrying out such adaptation, and thus proportioning the justification opportunity bits according to the variable frequency offset between the clock 0 and the clock 1, is called *synchronizer*.

2.2 Re-Synchronization of VCs in SDH Intermediate NEs

Let us consider, for example, the case of a SDH DXC where the VCs of incoming STM-*N* signals are cross-connected. Since each input signal is timed by the clock of the generating SDH node, the DXC must re-synchronize, according to the local equipment clock, all VCs before cross-connecting and retransmitting them in the output STM-*N* signals.

Referring again to Fig. 1, the VC mapping the PDH signal and timed by clock 1 is transported along the SDH chain by STM-*N* frames timed by the different clocks of the chain (clocks 2—*M*-1). In each node, the VC timed by clock 1 is re-synchronized to fit into STM-*N* frames, timed by a different clock, by means of *pointer justification*. Pointer justification allows to compensate in a NE the phase fluctuations between input VCs, carried in STM-*N* frames timed by the clock of the previous NE in the chain, and the output STM-*N* frames, timed by the local clock.

Re-synchronization of VCs is accomplished by means of an elastic store, in which VC bytes are written according to the timing signal extracted by the incoming STM-*N* signal and are read according to the local equipment clock. Pointer justification allows to compensate differences between the input and output frequencies. Therefore, this block based on an elastic store is called *pointer processor*.

2.3 Demapping of PDH Tributary from SDH Frames

The bits of the tributary extracted from the SDH frames do not arrive at a uniform rate, but according to a gapped clock. Therefore, demapping involves smoothing those gaps in order to return a regular bit stream.

Referring again to Fig. 1, the average frequency of the tributary returned at the end of the chain is, as obvious, the *same* as the original clock 0, except some residual jitter. In fact, regardless of what pointer action may happen along the chain, no bits are added or deleted from the tributary bit stream along its path!

The block performing the demapping of the tributary from its VC is called *desynchronize*r and fulfils the complementary function of the synchronizer. Its task is to reduce the jitter of the gapped clock timing the tributary extracted from STM-*N* frames.

3 Causes of Jitter and Wander in a SDH Transmission Chain

This section reviews the main causes of jitter and wander in a SDH transmission chain like that depicted in Fig. 1. The different phenomena affecting the phase of tributaries transported are outlined: variations of environmental conditions (temperature), inclusion of additional bits in the mapping of tributaries into the STM frames, bit and pointer justifications.

3.1 Variations of Environmental Conditions

Variations of temperature along the day and the year are a well-known cause of wander (*diurnal* and *annual wander*), since the first long-haul digital transmission systems have been set up. While this kind of wander was very important on long copper cable lines, its amplitude is far lower in optical fiber systems. Nevertheless, it may still reach several Unit Intervals (UI) of amplitude if the bit rate of the transmission system is high.

The most that can be done to reduce the wander effect of temperature variation is to bury the cable deep. This reduces the daily temperature variation to a fraction of a degree, although larger temperature swings will be seen annually. Moreover, diurnal and annual wander cannot be filtered out, owing to their extremely low frequency.

The main reason of such wander is that the propagation delay of the light in an optical fiber depends on the refractive index of the fiber core and on the fiber length, which both depend on the temperature. Hence, the digital signals exhibit different propagation delays during the day and the night, as well as during the winter and the summer. This mechanism yields a pseudo-periodical variation in the phase of the digital signal received, having period of about one day or one year (diurnal and annual wander).

More in detail, the propagation delay of an optical signal transmitted on an optical fiber of length l is given by [8][9]

$$t = \frac{l n_c}{c} \qquad (1)$$

where n_c is the group index of refraction of the fiber core and c is the light speed in the vacuum. It is evident that a slow change in l or n_c results in wander. Both optical fibre temperature changes and laser wavelength changes will

change n_c, while an optical fibre temperature change also results in a slight variation in the length of the optical fiber. Even a slight variation in temperature of the optical fiber can cause a significant amount of wander over a long distance, since both the group index of refraction and the length of the fiber are temperature-dependent.
Fluctuations in the laser transmitter wavelength are another source of wander in fiber optic systems. Wavelength variations cause wander because the group refractive index of the optical fiber is wavelength-dependent. Again, the drift in laser wavelength is mainly due to changes in laser temperature.
The Table 1 lists some typical values of dependence of the quantities mentioned above on the temperature, from reference [8] (in this table, J denotes the temperature and l the laser wavelength). Basing on such values, for example, the effect of a 1 °C fiber temperature change along a 1000 km transmission path containing 20 sections of 50 km each can be evaluated as about 40 ns of accumulated peak-to-peak diurnal wander, assuming that the temperature change is systematic along the entire route. In the case of a SDH STM-16 transmission system, having bit rate approximately equal to 2.5 Gb/s, this wander is equivalent to 100 UI.

$\partial n_c / \partial J$	1.2×10^{-5}/°C
$1/l \cdot \partial l / \partial J$	8.0×10^{-7}/°C
$1/c \cdot \partial n_c / \partial l$	$17\,\mathrm{ps/(nm \cdot km)}$ (at $l = 1.5$ì m)
$\partial l / \partial J$	0.1 nm/°C

Table 1: Typical values of optical fibre and laser characteristic quantities [8].

3.2 Overhead and Fixed Stuffing in the Mapping Structure

On designing the mapping of tributary signals into the STM-*N* frame, care was taken in dispersing the tributary bits along the frame. Nevertheless, the bits of the tributary extracted do not arrive at a uniform rate. The arrival rate of the bits of a certain tributary is given by a gapped clock signal, obtained from the regular clock associated to the incoming STM-*N* multiplex signal, by inhibiting the pulses corresponding to the unwanted bits (e.g. to miscellaneous overhead, fixed stuff, justification bits, etc.) [2].
The gapped clock associated to the mapped tributary is highly discontinuous. Its peak frequency is that of the regular STM-*N* clock, but, owing to its numerous gaps, its average frequency gets lower to that of the mapped tributary. The desynchronizer in the demultiplexing equipment smoothes its gaps thus returning a bit stream with regular clock at its average frequency.
The jitter of the mapped tributary gapped clock has very wide peak-to-peak amplitude, but it has most of its power at very high frequencies. Therefore, desynchronizers properly designed can cancel most of it. The residual jitter is very low and can be usually neglected compared to the jitter coming from other sources.

3.3 Bit Justification

The frequency offsets of plesiochronous tributaries are accommodated, on mapping into the synchronous Containers, by using the justification opportunity bits. The process of bit justification yields *waiting time jitter* [8][10]—[13]. This jitter, although of very low amplitude, is impossible to be filtered out completely by the output desynchronizer, owing to its unlimited low frequency, and can therefore accumulate along a chain of PDH-to-SDH and SDH-to-PDH mappings and demappings.
The overall jitter due to bit justification and to overhead and fixed stuff in the mapping structure, addressed in the previous section, is often referred to as *mapping jitter*.

3.4 Pointer Justification

The pointer-justification mechanism allows compensating in a NE the phase fluctuations between input VCs, timed by the clock of the originating NE in the transmission chain, and output STM-*N* frames, timed by the local clock. Each pointer adjustment shifts the VC back or forth in the carrier STM-*N* frame: a VC-4 is moved of three bytes, all other VCs are moved of one byte for each Pointer Justification Event (PJE). Therefore, who looks at the VC bits extracted from the incoming frame notices a sudden pause or acceleration in the bit flow after a pointer adjustment.
Said in a more formal way, the phase diagram of the VC digital signal exhibits a positive or negative step on each positive or negative pointer adjustment. The amplitude of the phase step corresponds to the number of bits justified by one PJE. In the case of the AU-4 pointer, one PJE justifies 24 bits of the VC-4, corresponding to about 160 ns. The bit flow of the demapped tributary exhibits a proportional phase step, corresponding to the number of tributary bits in the word justified. In the same case of the E4 mapped into the VC-4, the step amplitude may correspond to about 22 bits at the bit rate of 139.264 Mb/s.
This phase step in the demapped tributary digital signal is low-pass filtered by the desynchronizer, which smoothes it as a negative exponential curve, at least under the simple assumption of single-pole low-pass phase filter.

3.5 Experimental Results

To give an idea of how this residual phase hit looks, we report some measurement results obtained on a commercial SDH Line Terminal Multiplexer STM-16 (LTM-16).
The measurement set-up is depicted in Fig. 2. A STM-1 frame generator outputs a STM-1 signal (155.520 Mb/s) mapping a PDH E4 signal (139.264 Mb/s) via VC4. The STM-1 frame generator is also able to produce AU4 pointer adjustments in the frames generated, according to user-

defined patterns. Then, the STM-1 signal is sent to the tributary interface of a LTM-16, which sends it multiplexed in the line signal to a second LTM-16. The latter LTM-16 demultiplexes the E4 signal. A time counter then measures the phase deviation (jitter) between the demultiplexed E4 signal and its own built-in reference clock, which is also the test-bench master clock via a frequency synthesizer.

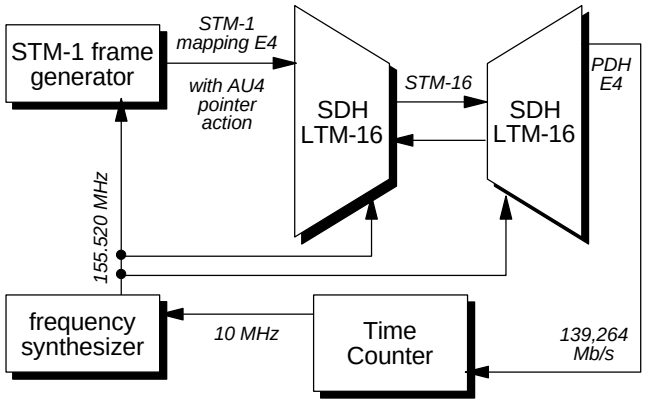

Fig. 2: Test bench for the measurement of output jitter due to AU4 pointer adjustments.

In this way, we are able to observe how the LTM-16 desynchronizer smoothes the phase hits resulting from AU4 pointer adjustments inserted by the STM-1 frame generator. Then, Fig. 3 reports the phase deviation plot [UI] measured over an interval of 10 s, with two series of four AU4 pointer adjustments occurring within this measurement interval. The amplitude of each step is about 22 UI (relative to the 139.264-Mb/s bit rate), while the time constant of the exponential transients is less than one second.

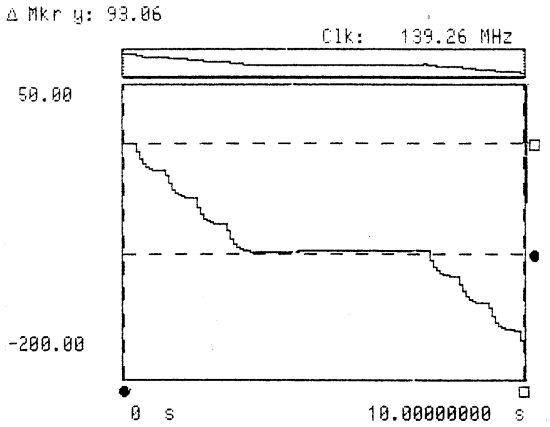

Fig. 3: Phase error [UI] between the demapped E4 and the carrying STM-*N* with series of four AU-4 pointer adjustments.

4 Conclusions

The bit and byte synchronization processes that take place in a SDH transmission chain were reviewed. In particular, mapping of PDH tributaries into SDH frames (by bit justification), re-synchronization of Virtual Containers (VCs) in intermediate nodes (by pointer justification) and demapping of PDH tributaries from SDH frames were described. Then, the main causes of jitter and wander in a SDH transmission chain were outlined: variations of environmental conditions (temperature), inclusion of additional bits in the mapping of tributaries into the STM frames, bit and pointer justifications. Real measurement results of phase hits caused by AU4 pointer adjustments were also provided, to show how the residual phase hits may look after the filtering action of a plain desynchronizer of a commercial SDH system.

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