Optical and Transport Networks

Prof. Stefano Bregni **I Exam 2023-24 – 11 January 2024**

Last and first name: *(capital letters)*

(signature)

Matriculation number:

NB: In any exercise, any answer not justified adequately, even with few words, will not be considered.

Problem 1

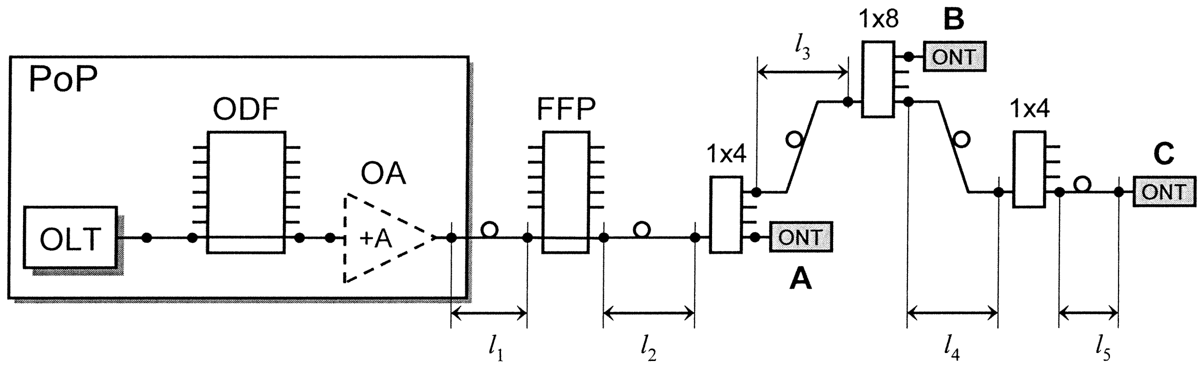
(Solve on this sheet in the space provided) (6 points)

Consider a Passive Optical Network reaching up to N users at variable distances from the Optical Line Termination (OLT) via a variable number of 1×4 and 1×8 splitters, with an asymmetric tree topology according to the scheme in figure.

The line from the OLT is cross-connected via an Optical Distribution Frame (ODF) to the PON. An Optical Amplifier (OA), if needed, may be added after the ODF at the Point-of-Presence (PoP). After a first single feeder fibre segment with length l_1, another ODF (Fibre Flexibility Point, FFP) cross-connects to the PON. The fibre segments between the FFP and the following splitters have length l_2, l_3, l_4, l_5, respectively. The length of other segments of fibres connecting network elements is negligible. The Optical Network Terminations (ONT) can be connected at the output of any splitter at the three stages (A, B, C).

Assume the following data for the PON elements:

- fibre with attenuation $\alpha = 0.25$ dB/km;
- $l_1 = 4$ km, $l_2 = 4$ km, $l_3 = 2$ km, $l_4 = 2$ km, $l_5 = 10$ km;
- OLT transmission power $P_{TX} = 250$ μW;
- splitter insertion loss $\alpha_s = 1$ dB;
- power loss by each couple of optical connectors $\alpha_c = 0.5$ dB (connections marked with dots in figure);
- sensitivity of ONT receivers $P_{RX} > -33$ dBm, with at least 6 dB of safety margin to be guaranteed;
- optional OA gain $+A$ [dB] (excluding the additional attenuation $2\alpha_c$ introduced by its two couples of connectors);



a) Evaluate the maximum *Differential Path Loss* [dB] between ONTs.

b) Evaluate the power P_{RX} [W] received by the farthest ONT in position C without OA.

c) Determine if it is necessary to add an OA, to make the power P_{RX} received by the farthest ONT not less than the minimum power required at the ONT receiver.
   - If the OA is necessary, calculate the minimum OA gain (excluding the additional attenuation $2\alpha_c$ introduced by its two couples of connectors) required.
   - Otherwise, if the system is feasible without OA, calculate the maximum length L of the last fiber segment, to have P_{RX} at any ONT not less than the sensitivity of receivers including the safety margin.

d) The OLT transmits a square timing signal downstream to synchronize all ONTs, which are equipped with PLL-based slave clocks. Can ONTs be synchronized on the same absolute time? Their relative *Time Error*, between any pair, will constant or variable, disregarding any jitter?

a) $\max DPL = P_{Rx/A} - P_{Rx/C}$ [dB]

$$= \alpha(l_3 + l_4 + l_5) + 5\alpha_c + (\alpha_s + 9) + (\alpha_s + 6) = 23 \text{ dB}$$

b) $P_{Rx/c} = P_{Tx} - 12\alpha_c - (\alpha_s + 9) - 2(\alpha_s + 6) - \alpha \sum_1^5 l_i$ [dB]

$= -41{,}5$ dBm $= 71$ nW $\qquad P_{Tx} = -6$ dBm

c) $P_{Rx/c} < -27$ dBm $\Rightarrow$ OA

$A \geq 14{,}5 \text{ dB} + 2\alpha_c = 15{,}5$ dB

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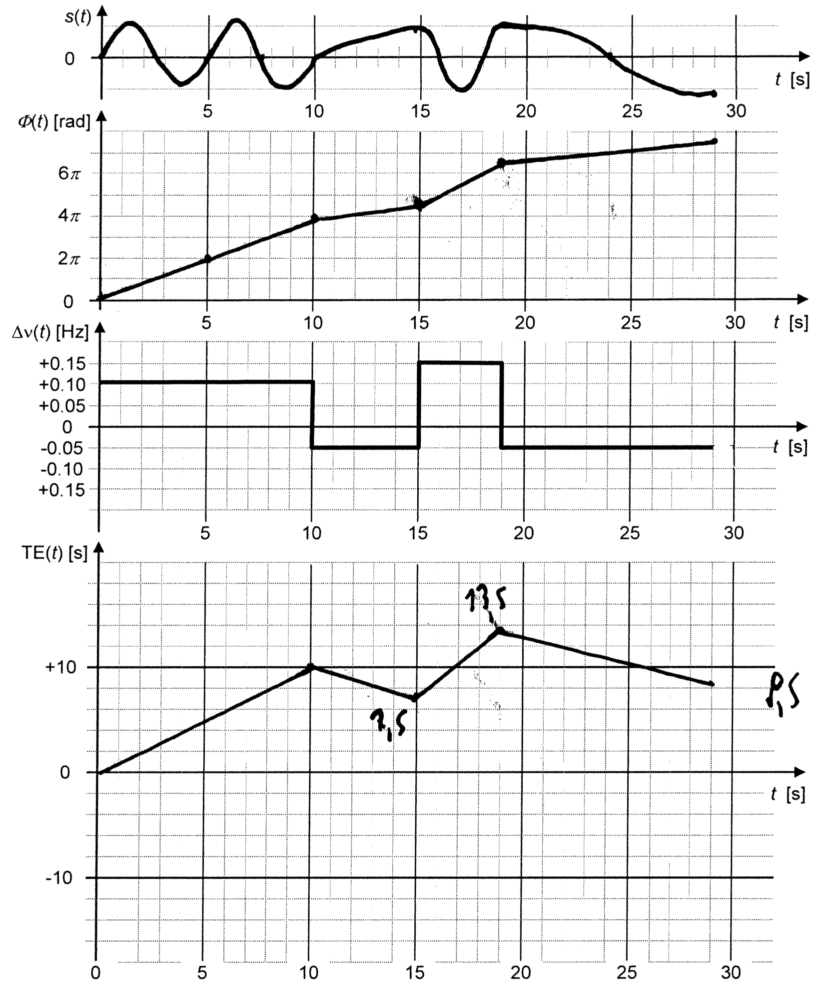
Problem 2

(Solve on this sheet in the space provided) (8 points)

a) Let $s(t)$ be a pseudo-sinusoidal timing signal with nominal frequency $\nu_0 = 0.1$ Hz and *instantaneous frequency error* $\Delta\nu(t) = \nu(t) - \nu_0$ as plotted in figure.

Where possible, plot on the graphs at right:

- the timing signal $s(t)$;
- the *Total Phase* $\Phi(t)$ of $s(t)$ and of the ideal timing signal with frequency ν_0, both starting from $\Phi(0) = 0$;
- the *Time Error* TE(t) with respect to an ideal timing signal with frequency ν_0, starting from TE(0)=0, with the convention that positive TE denotes time advance.



$T_0 = \frac{1}{\nu_0} = 10$ s

b) Let $s(t)$ be a non-ideal timing signal generated by a clock with initial instantaneous frequency set to the nominal frequency $\nu(0) = \nu_0 = 1$ MHz and coefficient of linear frequency drift $D = +10^{-6}$/week.

Under the assumption that the frequency drift remains linear with coefficient D indefinitely, evaluate the *Time Error* TE(t) [s] measured by this clock at $t = 10$ days with respect to an ideal timing signal with constant frequency ν_0 and same phase at $t = 0$.

$T(t) = \frac{\Phi(t)}{2\pi\nu_0} = t + \frac{D}{2}t^2$

$TE(t) = T(t) - t = \frac{D}{2}t^2$

For $t = 10$ days:

$TE(10\,d) = \frac{1}{2} 10^{-6} \frac{1}{7}/\text{day} \cdot 10^2\ \text{days}^2 = \frac{1}{14} \cdot 10^{-4}\ \text{days} = 0{,}617$ s

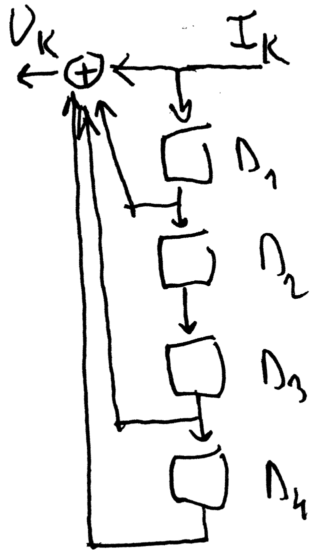
Problem 3

(Solve on this sheet in the space provided) (6 points)

a) Draw the scheme of a *self-synchronizing descrambler* with characteristic polynomial $P(x) = x^4 + x^3 + x + 1$.

b) Initialize the delay cells D_i (i = 1, 2, 3, 4) as {1, 0, 0, 0} at the initial step k = 0. Feed it with the bit sequence to descramble $\{I_k\}$ = {1, 1, 1, 0, 0, 0, 1, 1, 1, 0, 0, 0, …} (periodic). Calculate the descrambled bit sequence $\{U_k\}$.

a)



K	I_k	D_{1k}	D_{2k}	D_{3k}	D_{4k}	U_k
0	1	1	0	0	0	0
1	1	1	1	0	0	0
2	1	1	1	1	0	1
3	0	1	1	1	1	1
4	0	0	1	1	1	0
5	0	0	0	1	1	0
6	1	0	0	0	1	0
7	1	1	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	

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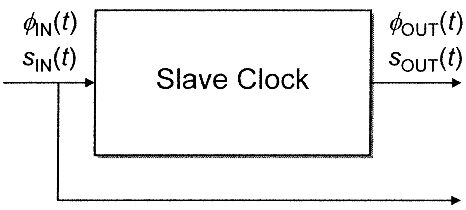
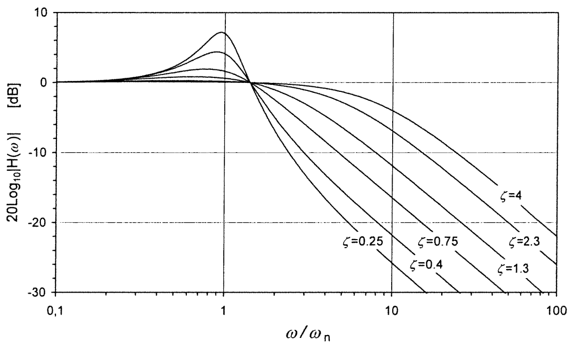
Problem 4

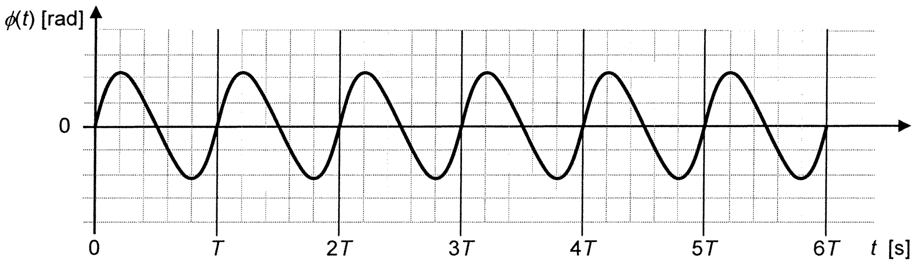
(Solve on this sheet in the space provided) (16 points)

1) Consider a Slave Clock based on a *second-order PLL* system, as shown in the figure below at left. Let us denote as $s_{IN}(t)$ and $s_{OUT}(t)$ its input and output timing signals, respectively, and as $\phi_{IN}(t)$ and $\phi_{OUT}(t)$ their respective *phase errors* vs. the Total Phase $\Phi(t)$ of the ideal timing signal $s(t) = A \sin 2\pi\nu_0 t$ considered as common reference in this model, having frequency ν_0. Therefore: $s_{IN}(t) = A \sin(\, 2\pi\nu_0 t + \phi_{IN}(t)\,)$ and $s_{OUT}(t) = A \sin(\, 2\pi\nu_0 t + \phi_{OUT}(t)\,)$. The closed-loop transfer function of the PLL is the standard $H(s)$ plotted below at right ($\omega_n = 20\pi\ \mathrm{s}^{-1}$, $\zeta = 0.25$). *(4 points)*

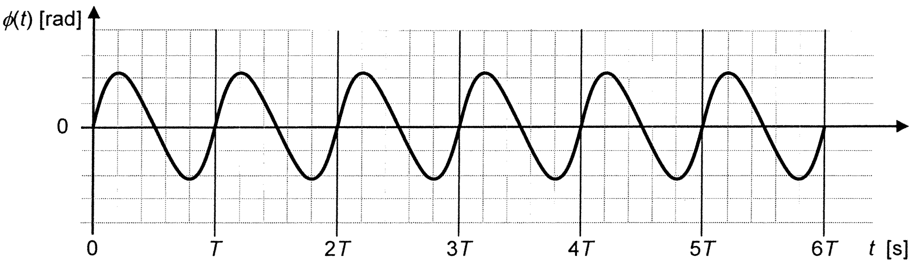




The input timing signal $s_{IN}(t)$ exhibits a phase error $\phi_{IN}(t)$ vs. the Total Phase of the ideal timing signal $s(t)$ as shown in the graphs below (sinusoidal). Plot on the same graphs the output phase $\phi_{OUT}(t)$ ignoring the initial phase alignment between input and output. Explain and express your considerations.



$T = 100$ ms



$T = 1$ s

2) Define what are *forced loss of alignment*, *real loss of alignment*, *fake alignment*. Explain when they occur and how to avoid them. *(3 points)*

3) Define the *packet jitter* of a sequence of packets transmitted with constant rate over a network. Propose a way to cancel or reduce it on the output data stream. *(3 points)*

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4) What is interleaving in *Bit Interleaved Parity* codes BIP(n,m)? What is its purpose? What is a reasonable criterion to determine the interleaving depth n? *(3 points)*

5) Describe an experimental set up and procedure to measure the *Time Error* between a Clock Under Test (CUT) and a Reference Clock (RC). *(3 points)*